

Foxconn Precision Co. Inc.

G41M01 Schematic

Fab.A
Data: 2008/7/15

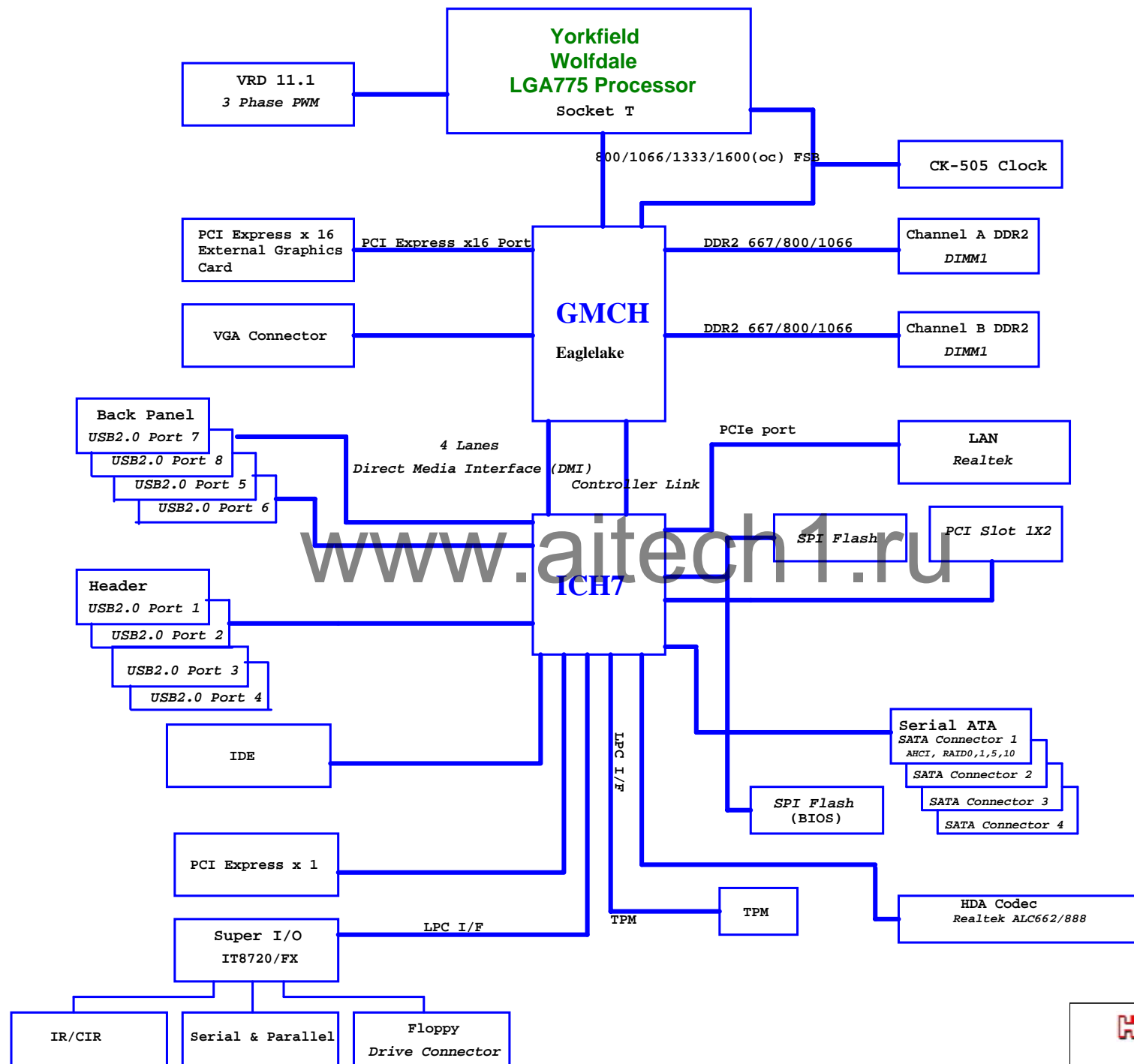
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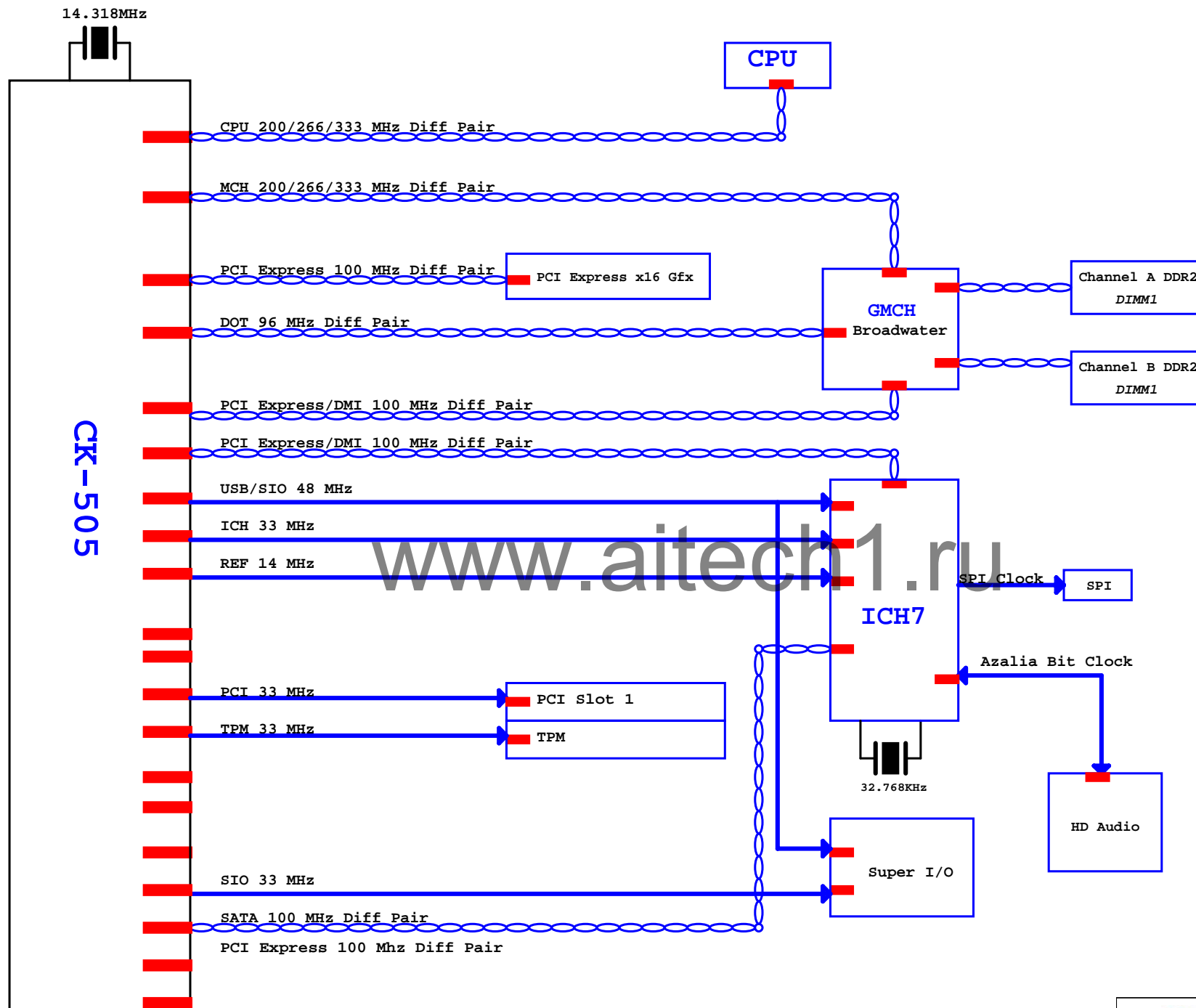
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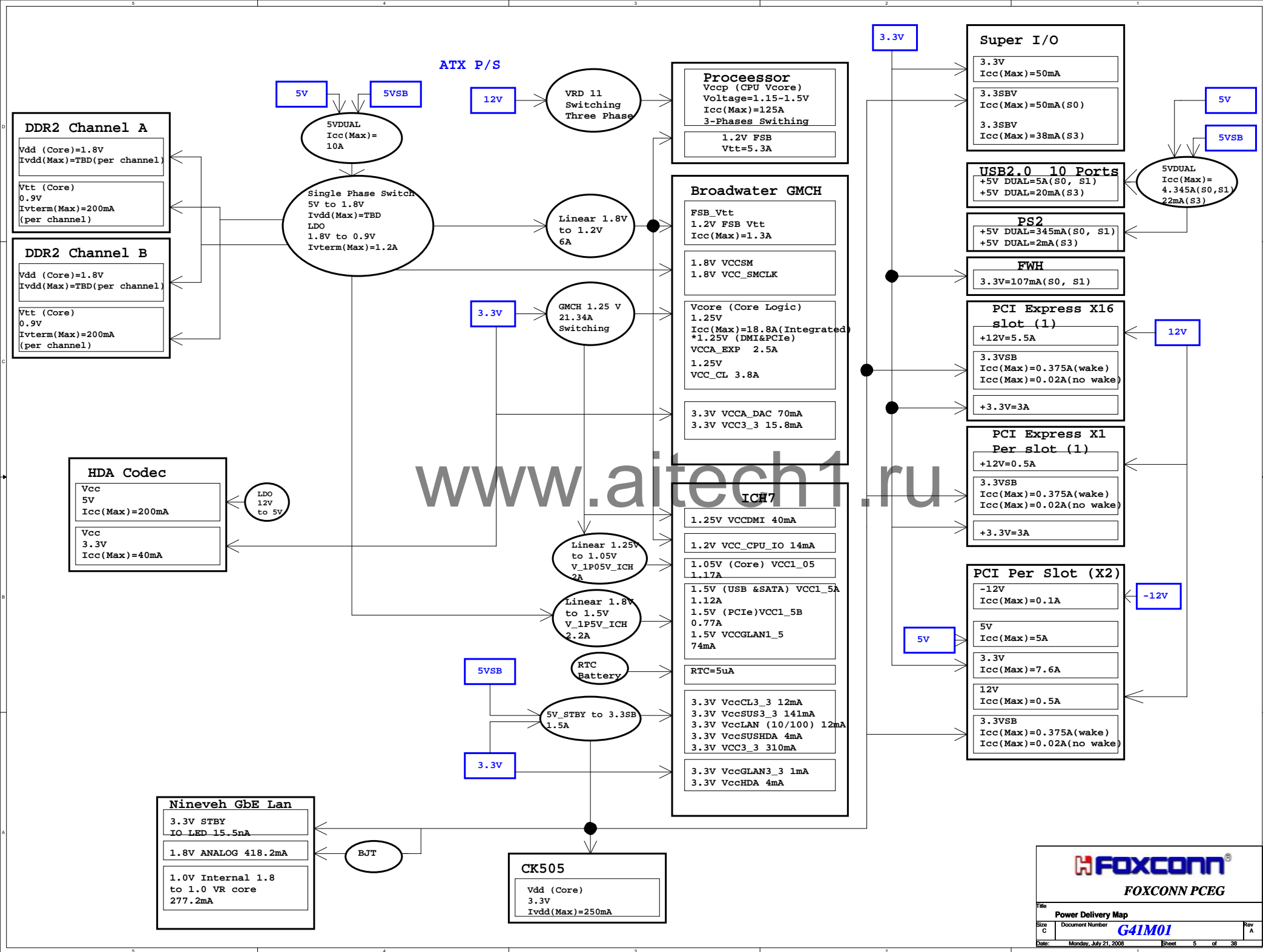
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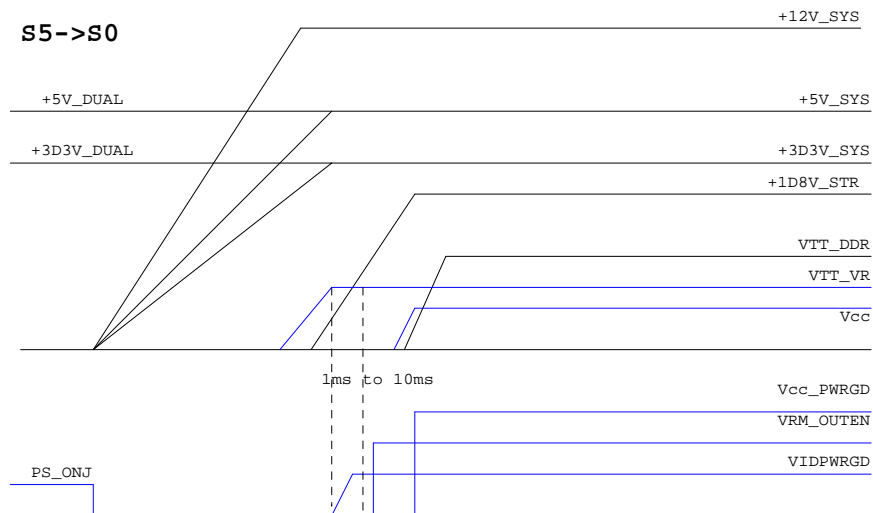
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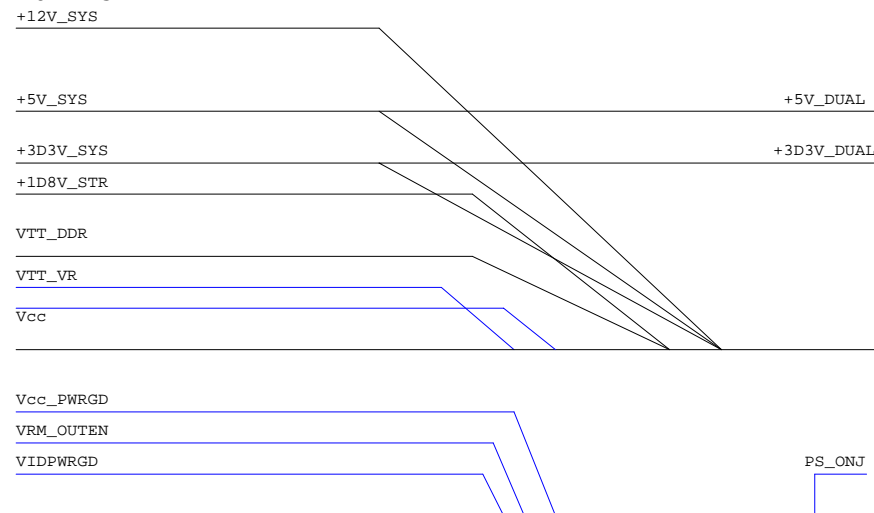




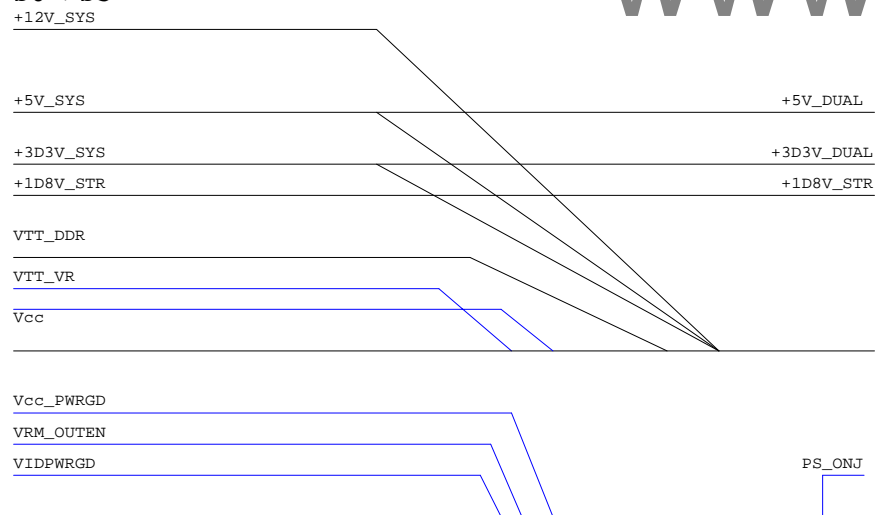
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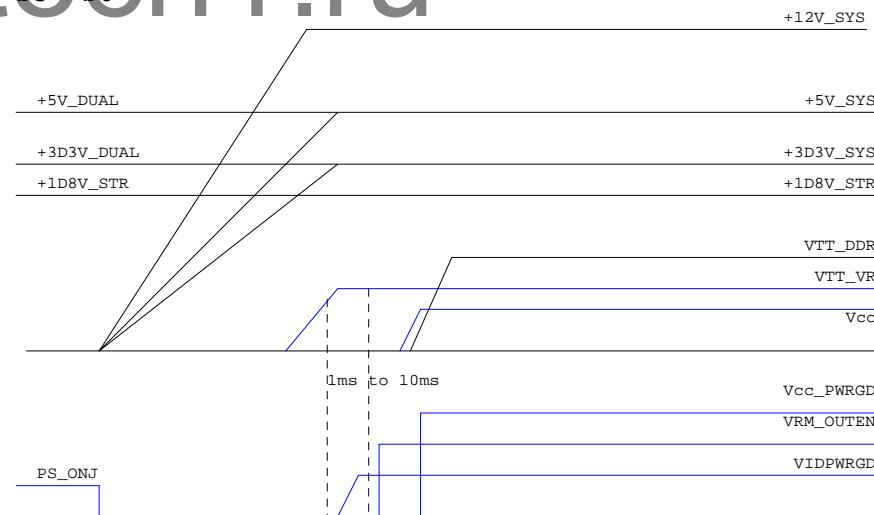
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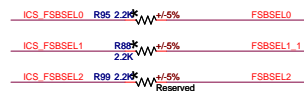
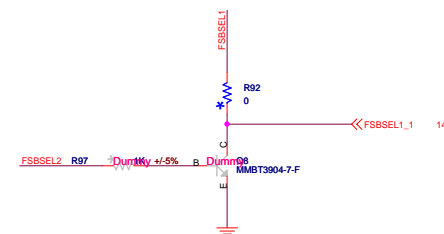
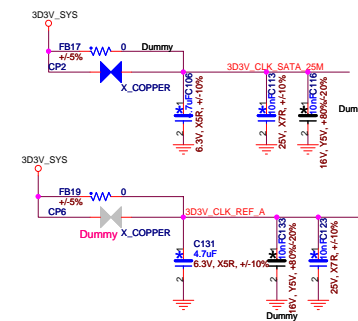
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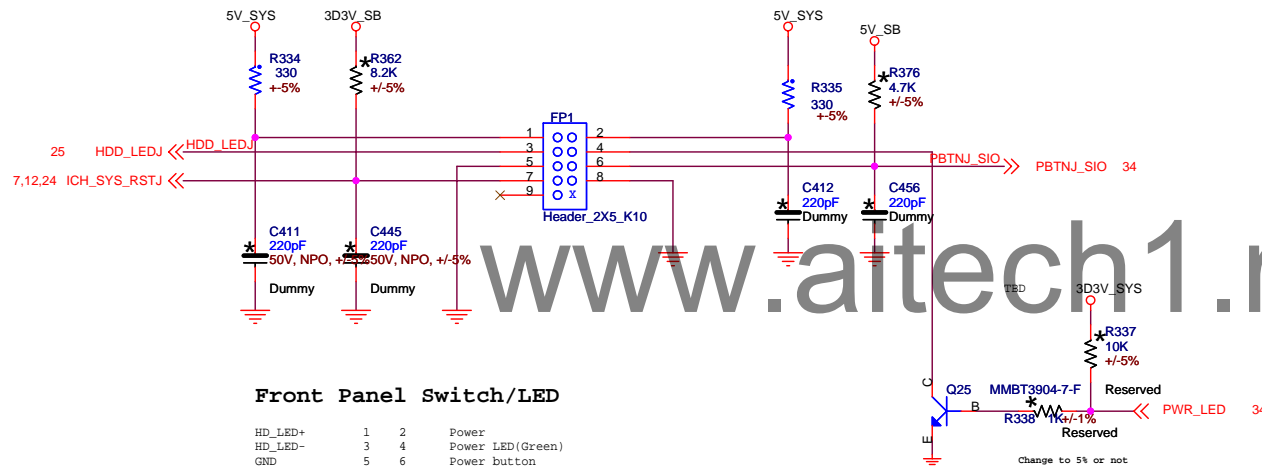
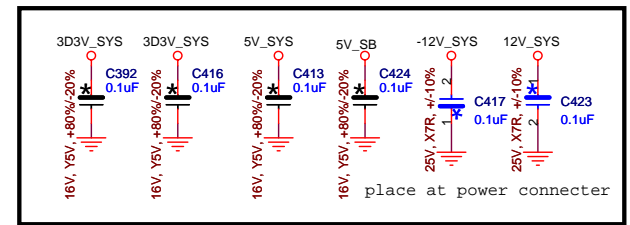
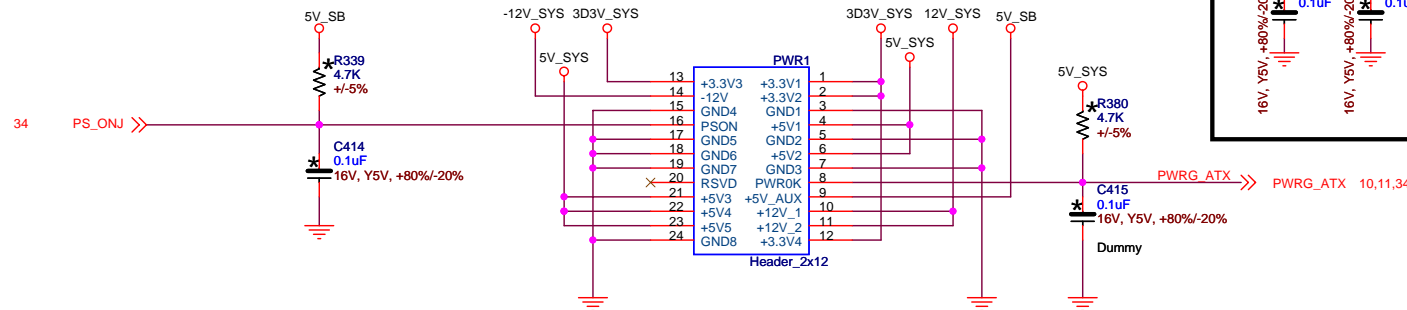
S3->S0



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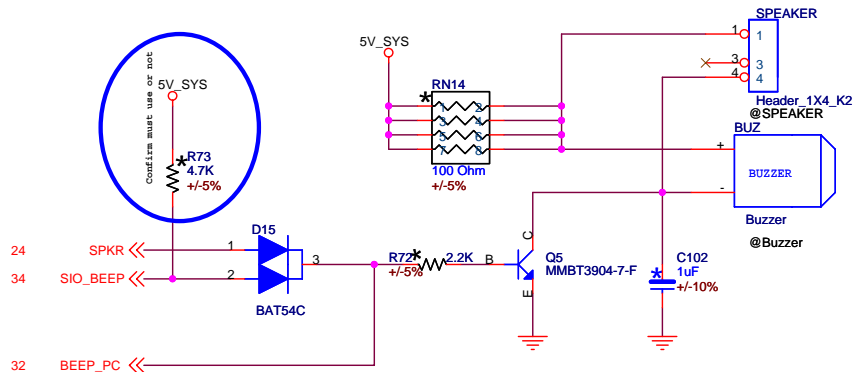
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Front Panel Switch/LED

HD_LED+	1	2	Power
HD_LED-	3	4	Power LED(Green)
GND	5	6	Power button
Reset button	7	8	Power
NC	9	10	Key

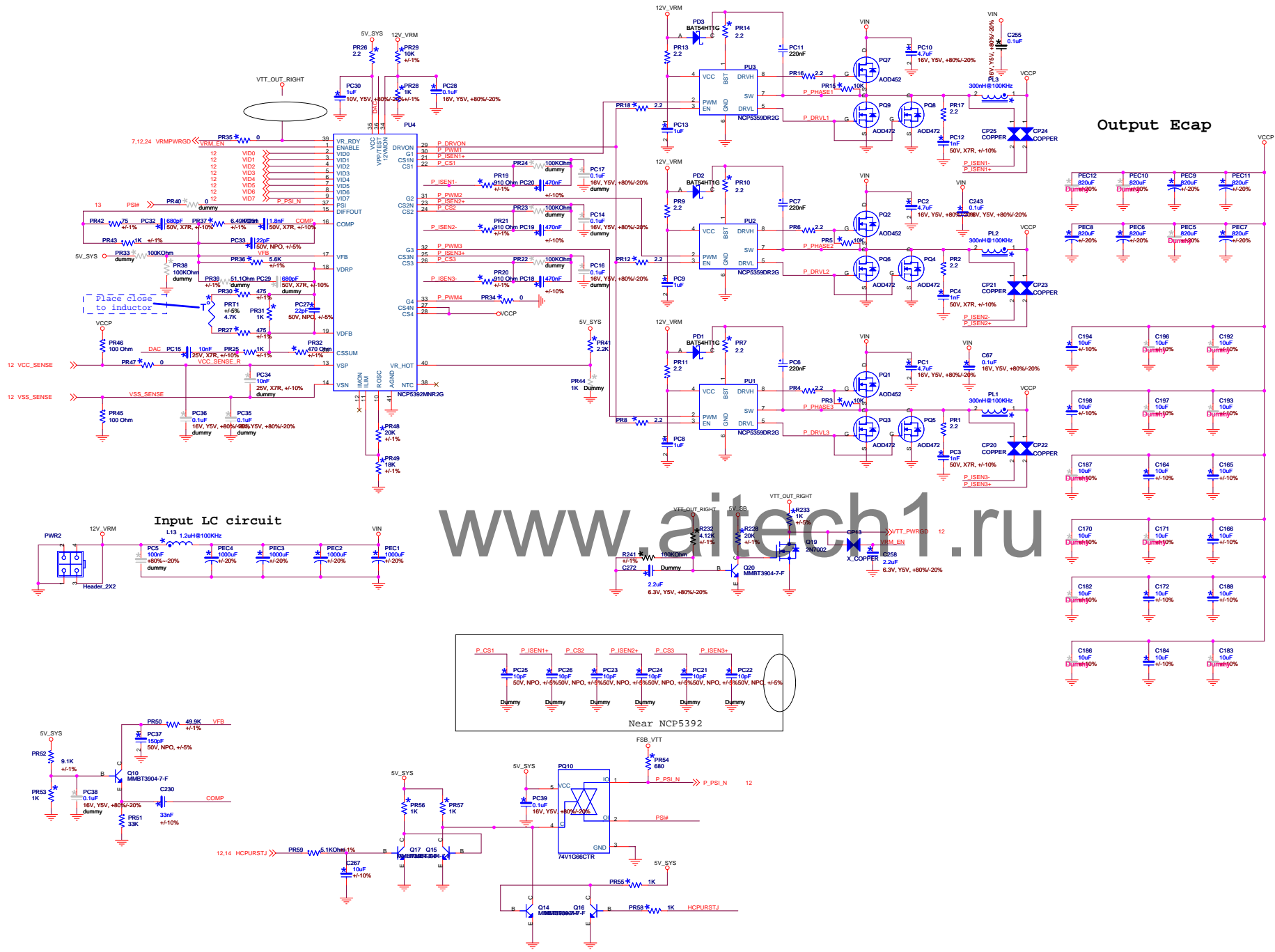
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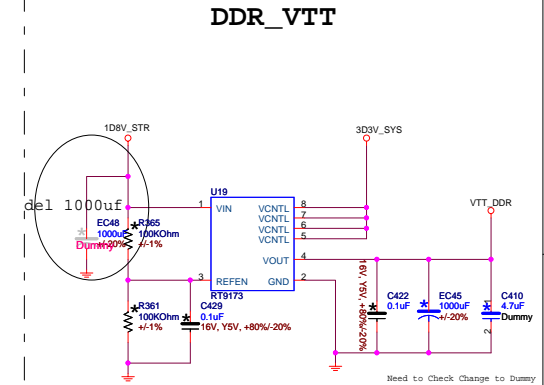
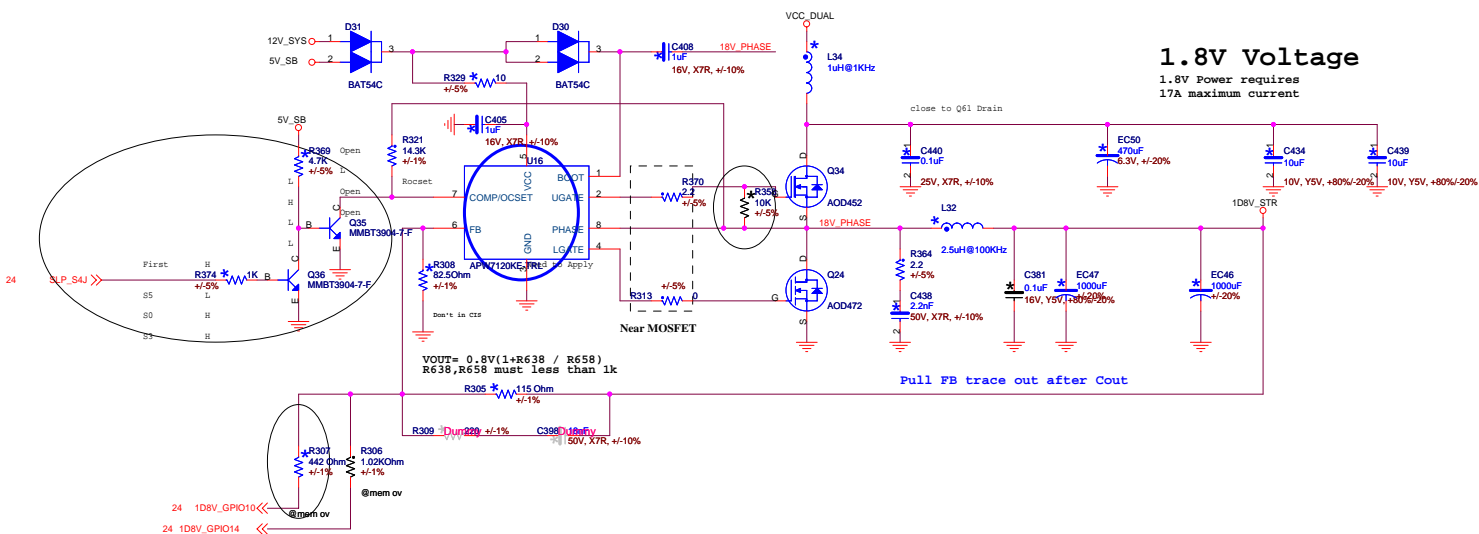
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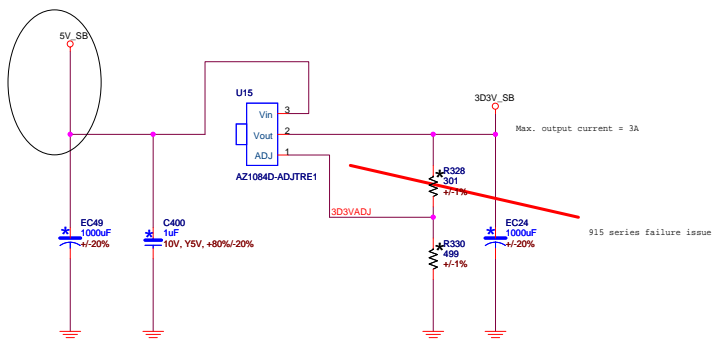


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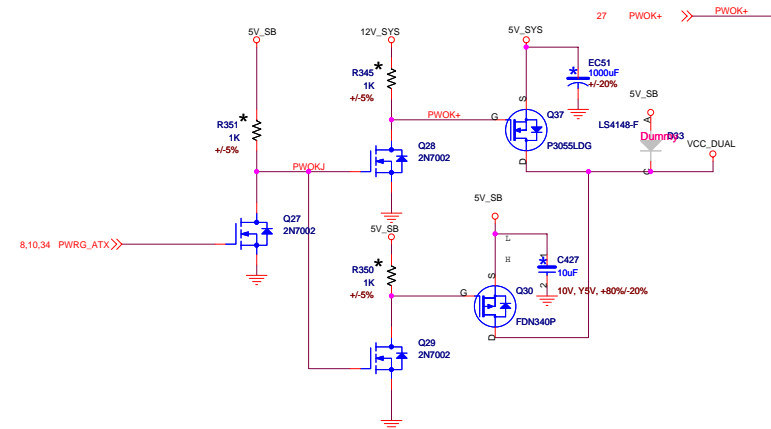
1D8V_STR

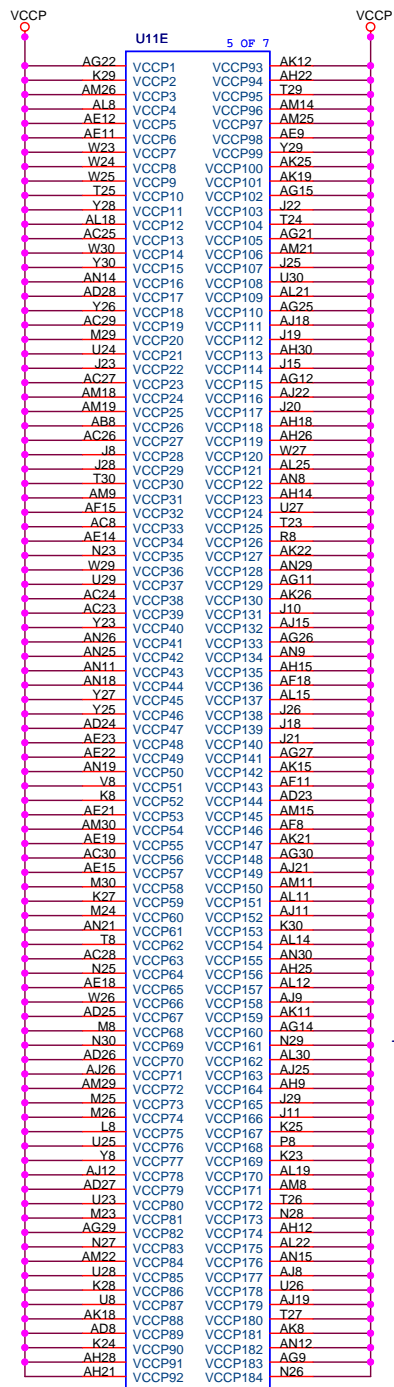
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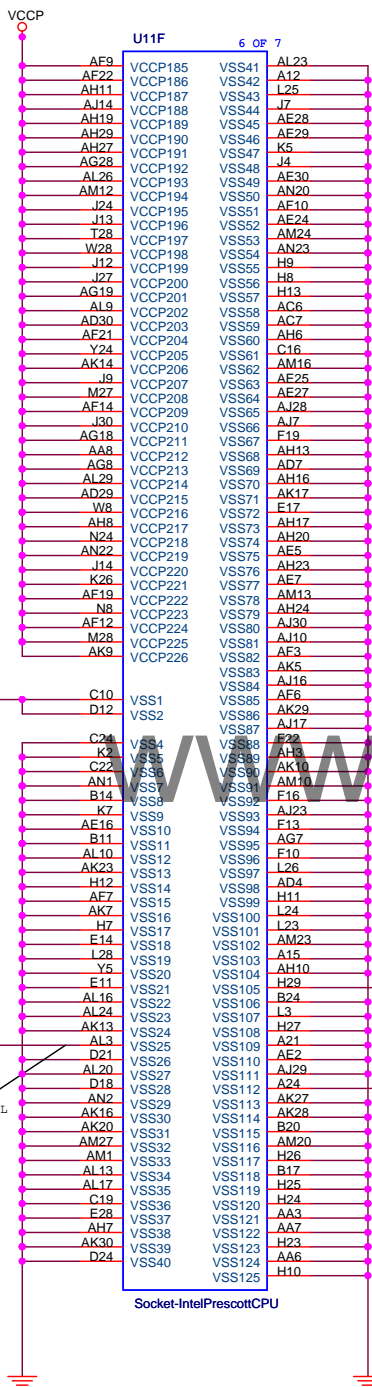
$$V_{out} = V_{ref}(1 + R2/R1) + I_{adj}R2$$

R1 is Up Resistor.
Iadj = 50uA
Vref = 1.25V

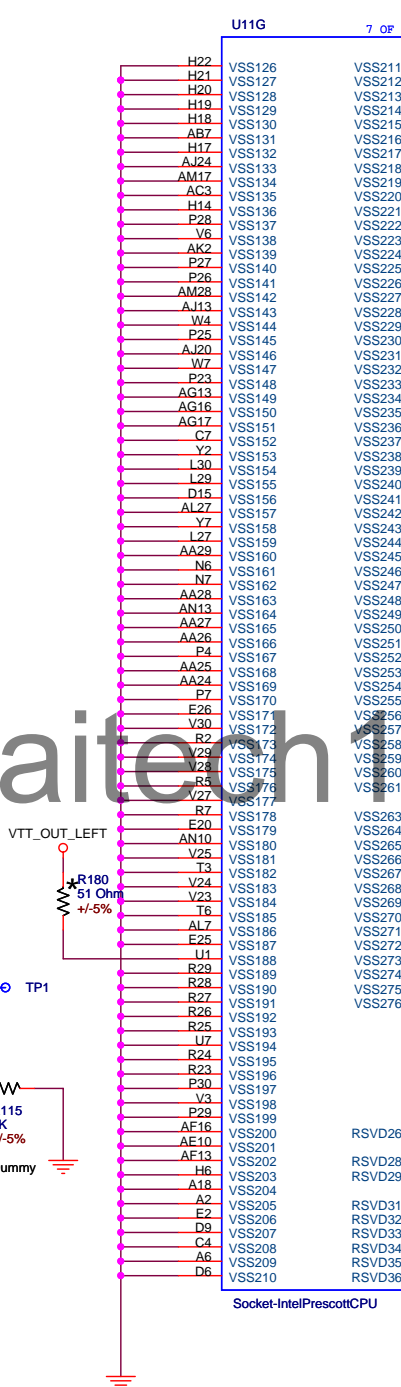




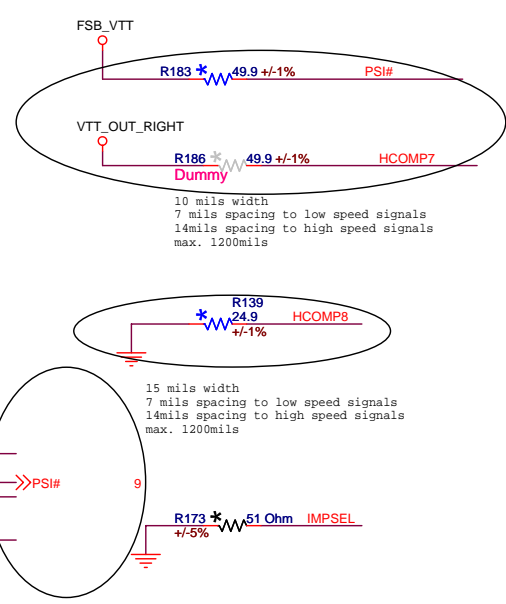
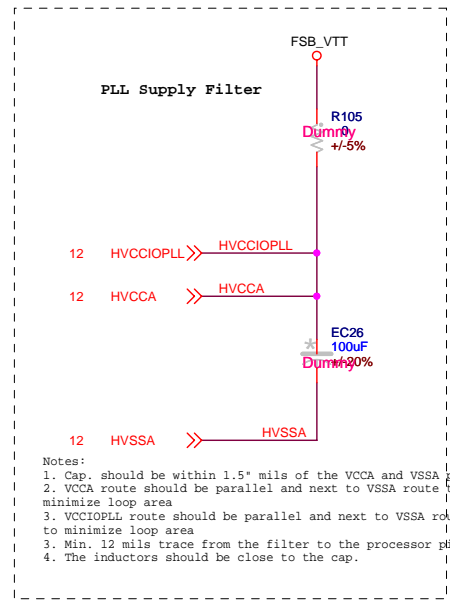
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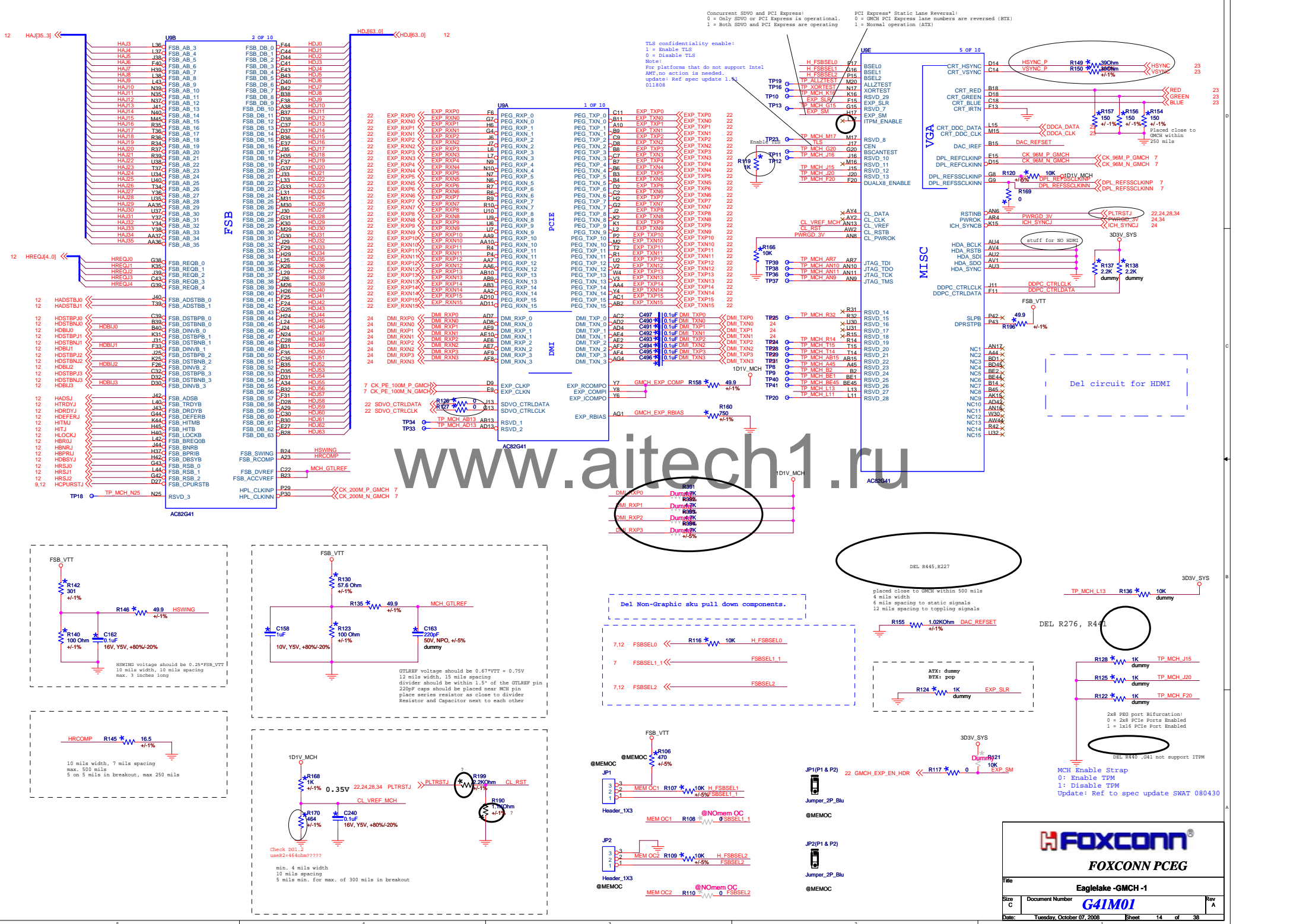


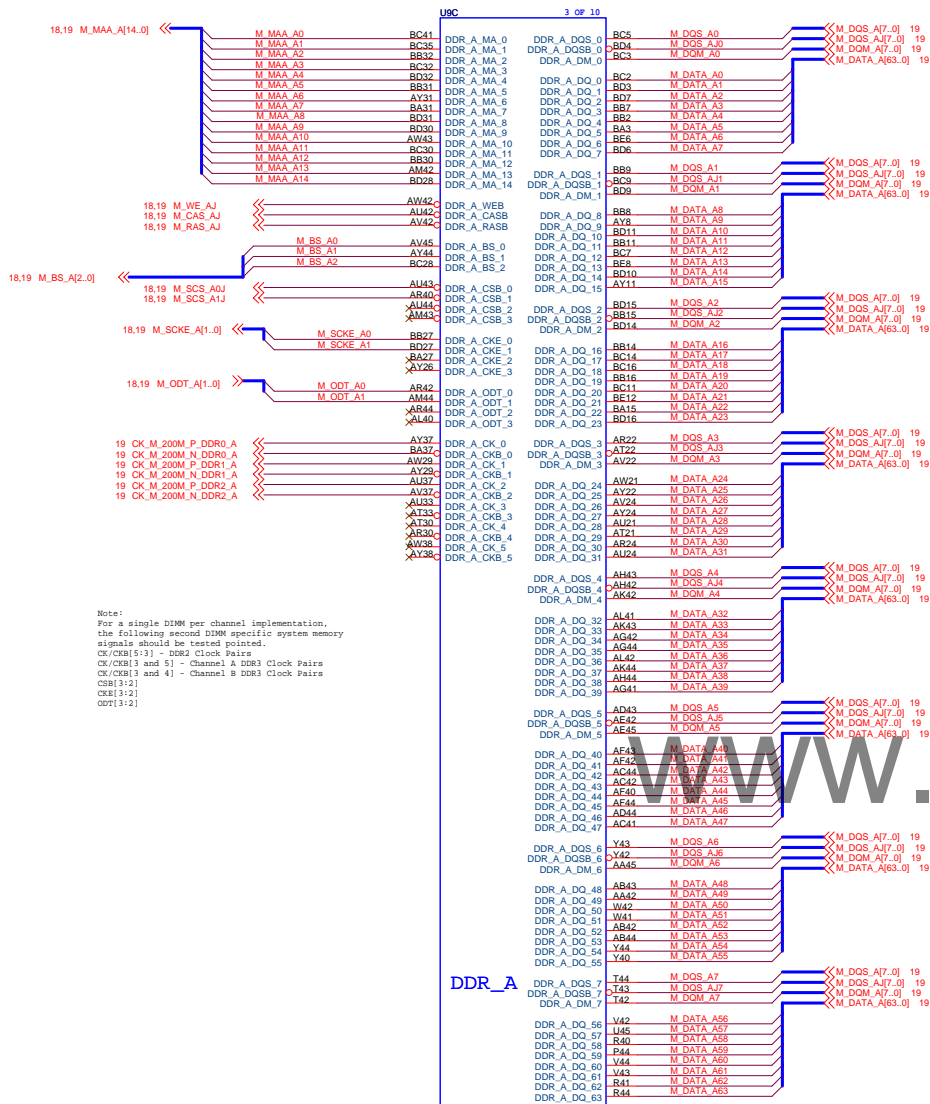
Socket-IntelPrescottCPU



Socket-IntelPrescottCPU



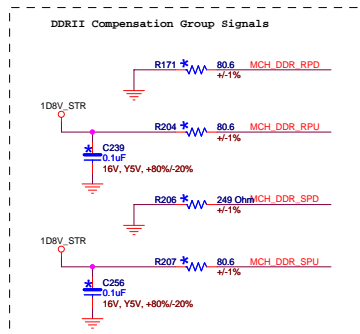
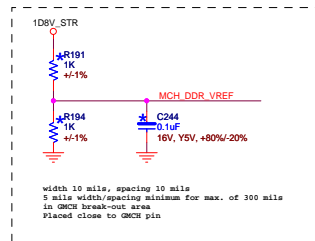




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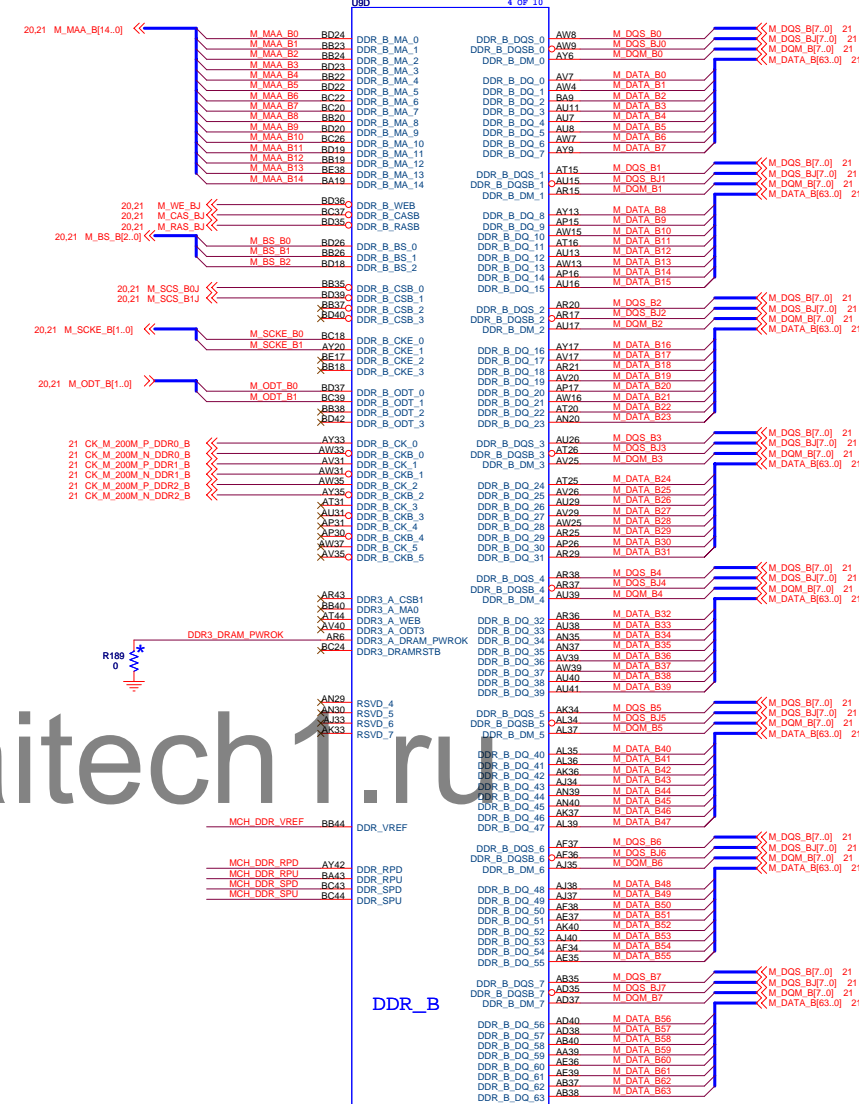
AC82G41

Note:
For a single DIMM per channel implementation,
the following second DIMM specific system memory
signals should be tested pointed:
CK/CB[5:3] - DQS2 Clock Pairs
CK/CB[3 and 5] - Channel A DQS3 Clock Pairs
CK/CB[3 and 4] - Channel B DQS3 Clock Pairs
CSB[3:2]
CSB[3:2]
ODT[3:2]



DDR_B

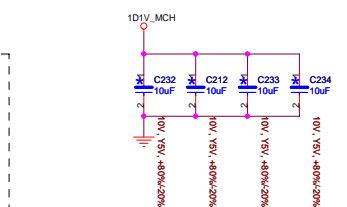
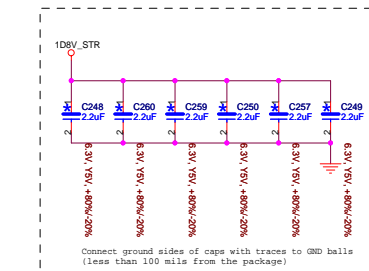
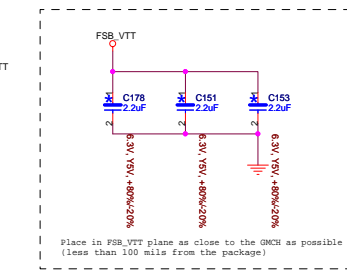
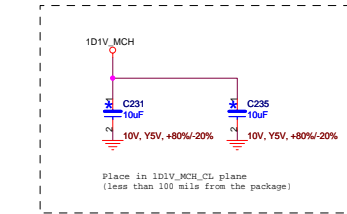
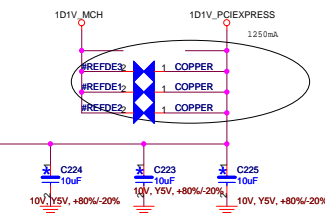
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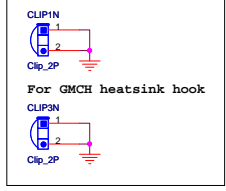
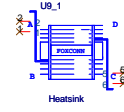
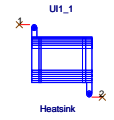
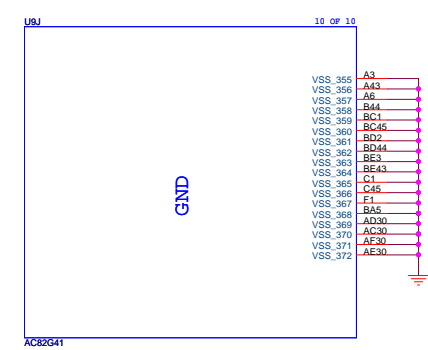
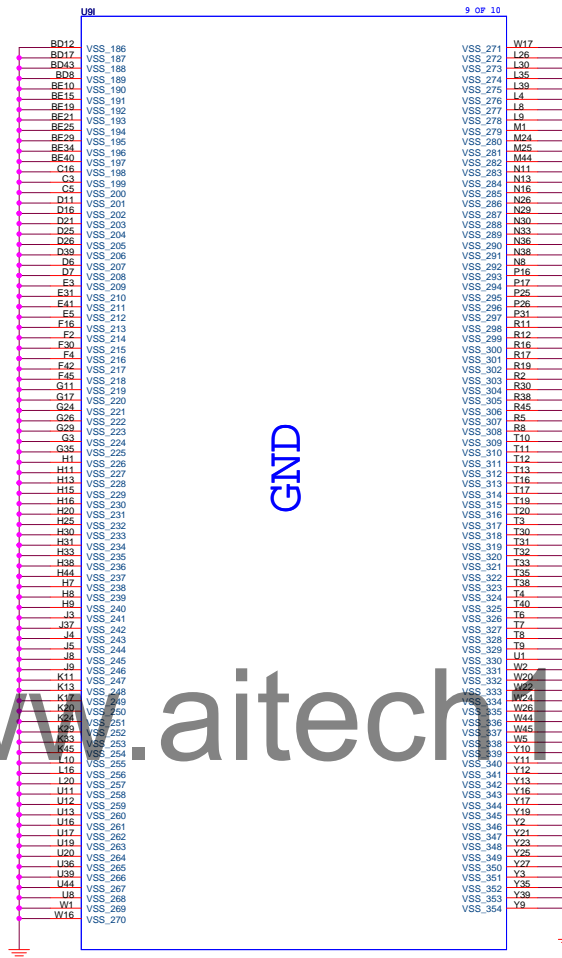
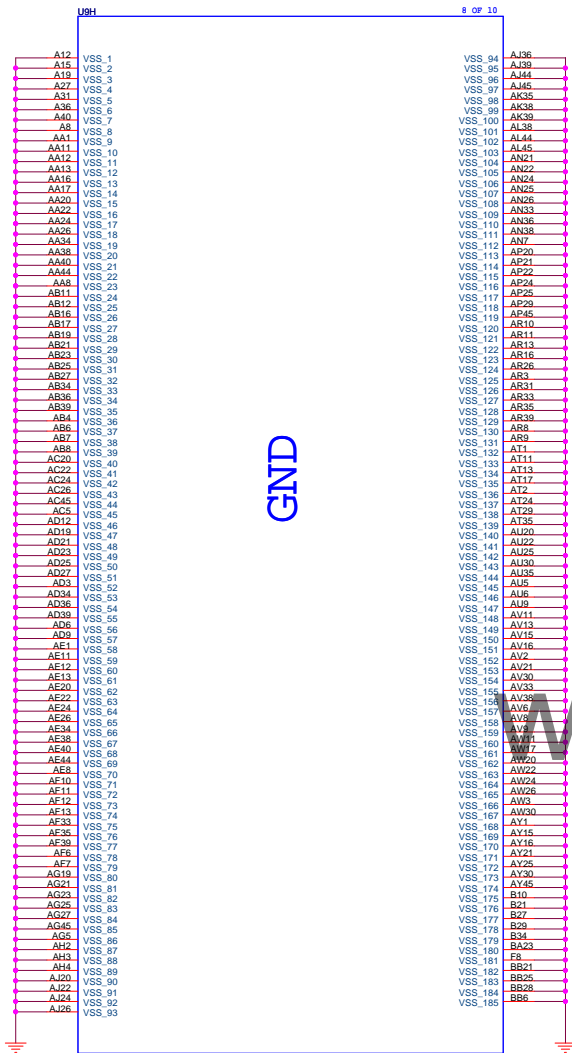
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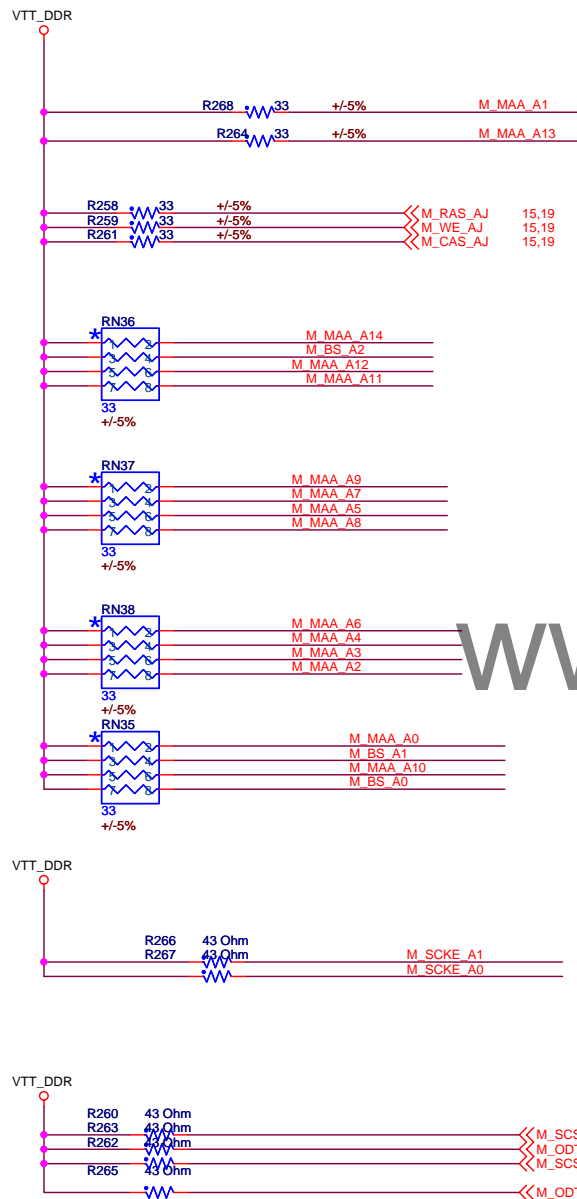
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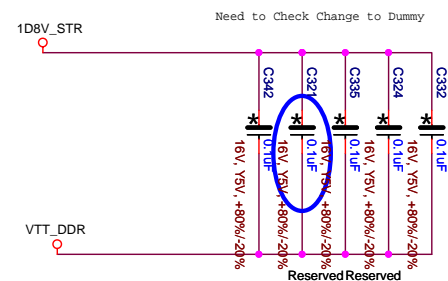
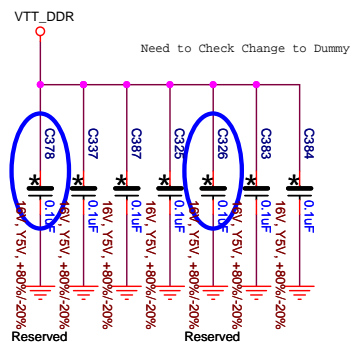


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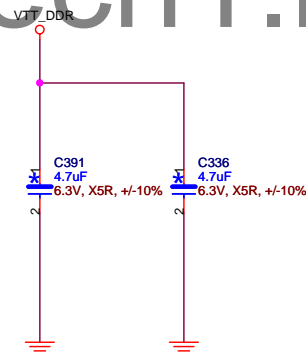




<<M_ODT_A[1..0] 15,19
 <<M_SCKE_A[1..0] 15,19
 <<M_BS_A[2..0] 15,19
 <<M_MAA_A[14..0] 15,19

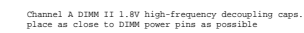
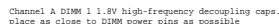
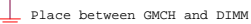
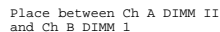


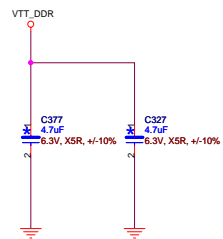
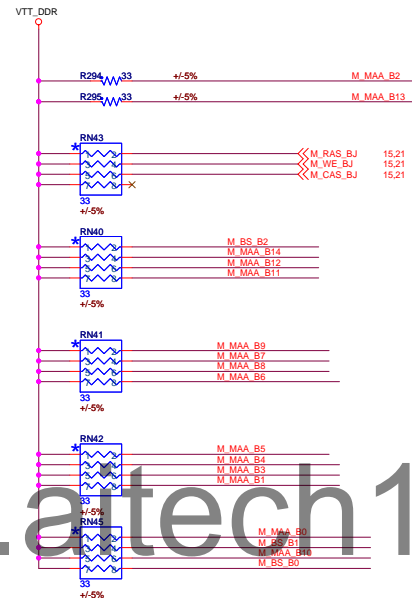
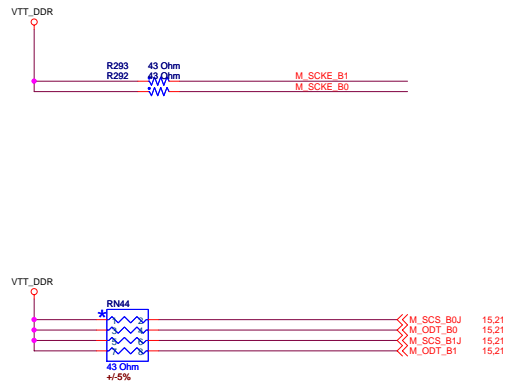
Channel A VTT_0.9V high-frequency decoupling caps.
Place as close to termination resistors as possible



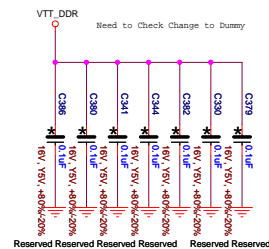
Channel A VTT_0.9V Mid Range decoupling caps.
Placed in termination Island

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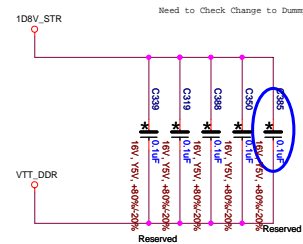


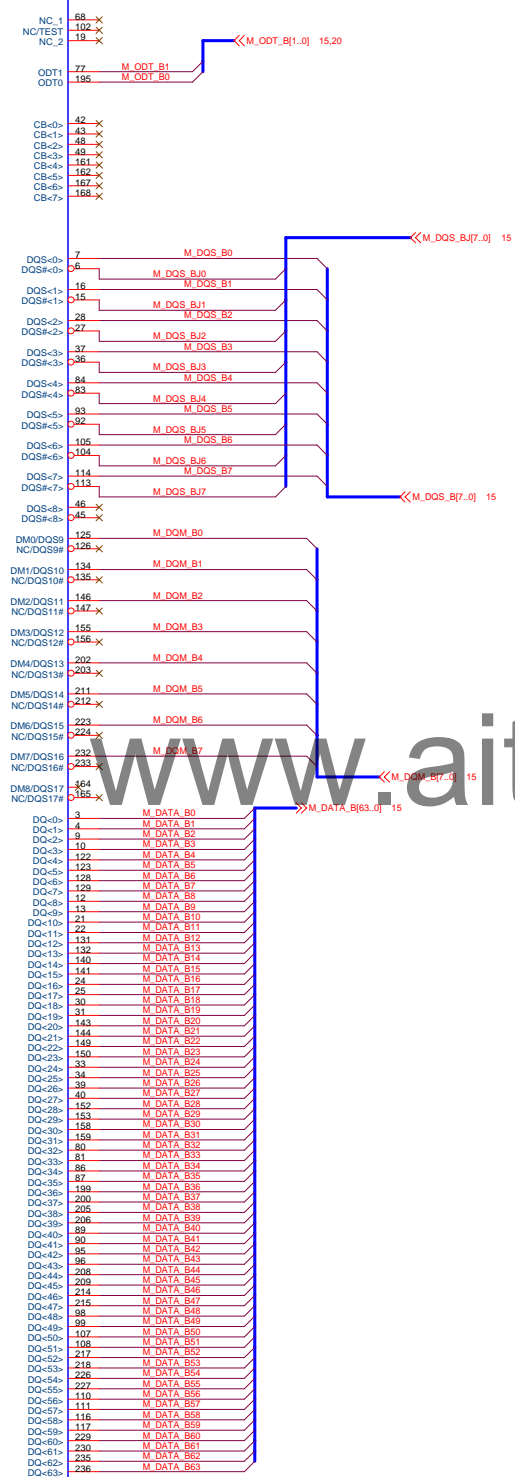
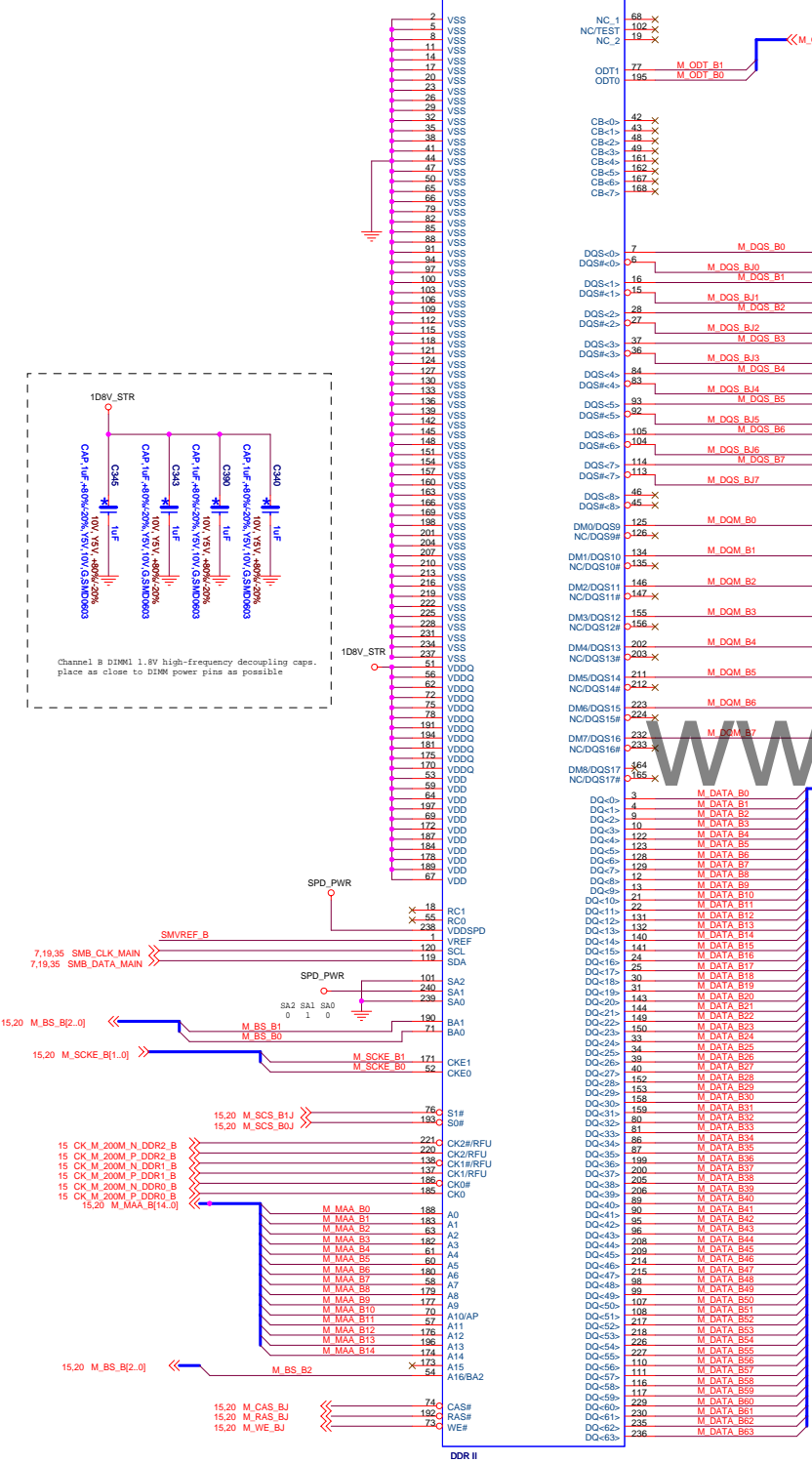
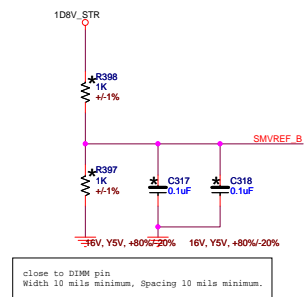
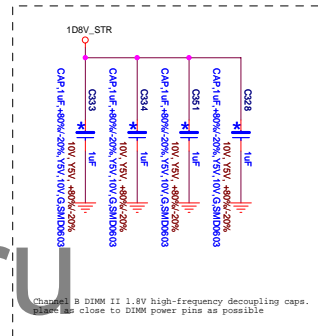
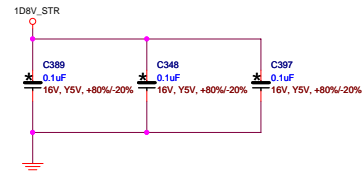
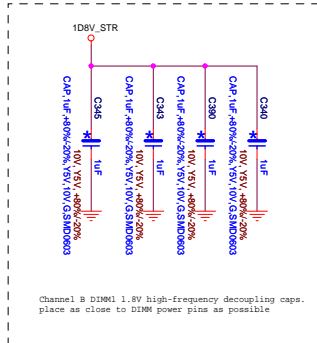


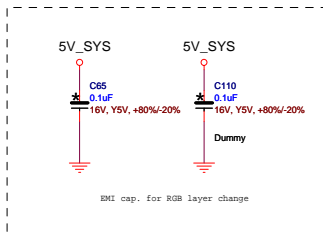
Channel B VTT_0.9V Mid Range decoupling caps.
Placed in termination Island



Channel B VTT_0.9V high-frequency decoupling caps.
Place as close to termination resistors as possible

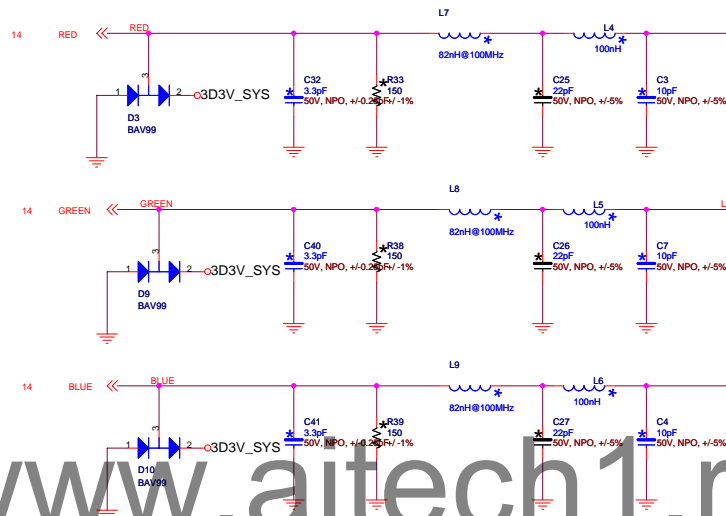
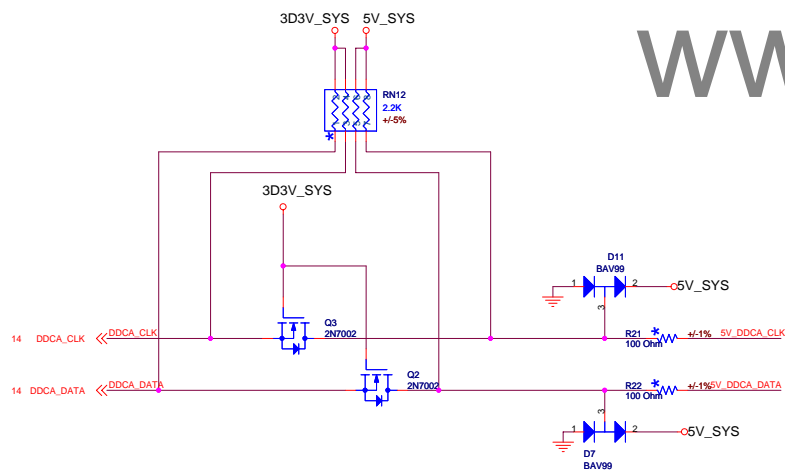




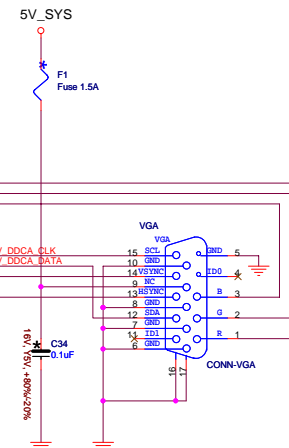
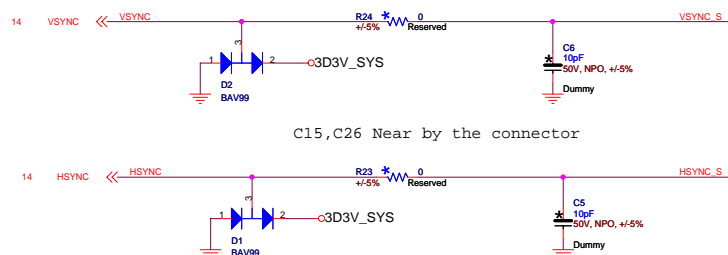
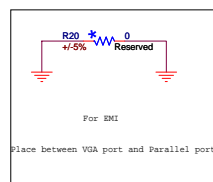


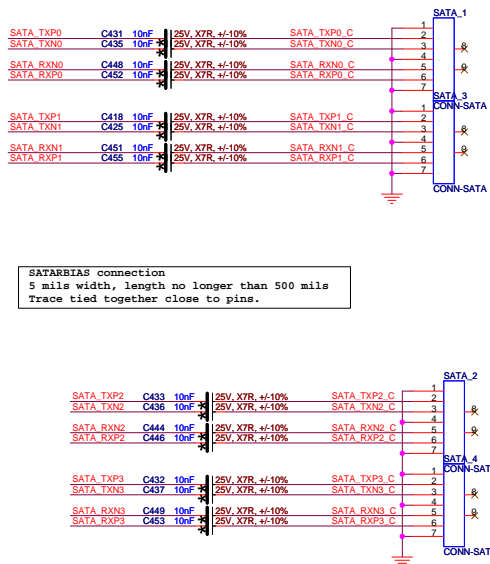
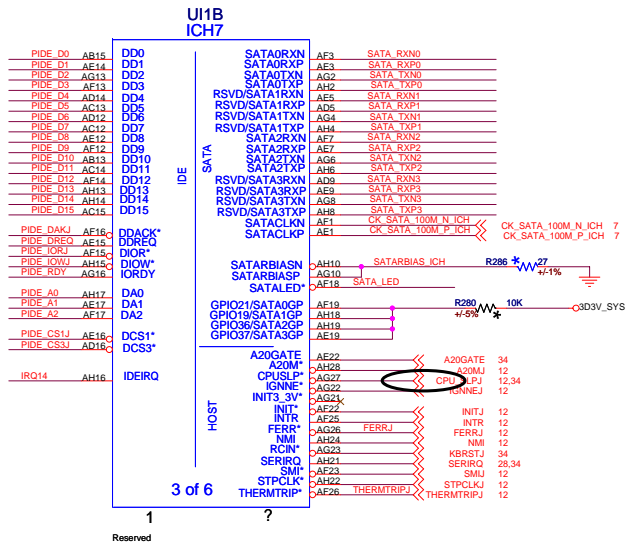
RGB routing

1. from GMCH to the first 150 ohm resistor: 7.5 mils(min. 6 mils spacing)
2. from the first 150 ohm res. to the second 150 ohm resistor: 4 mils
3. from the second 150 ohm resistor to connector: 4 mils
4. spacing minimum 6 mils, 30 mils spacing is recommended
5. R,G,B should be length matched to 700 mils, max. length is 8400 mils
6. R,G,B signals should be ground referenced

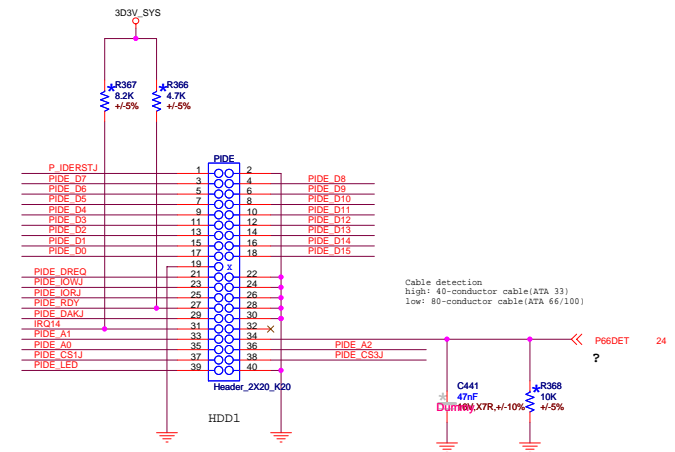


The 150 Ohm resistors near VGA connector and minimizing length to filter. The filters to VGA connector maximum distance 800 mils.

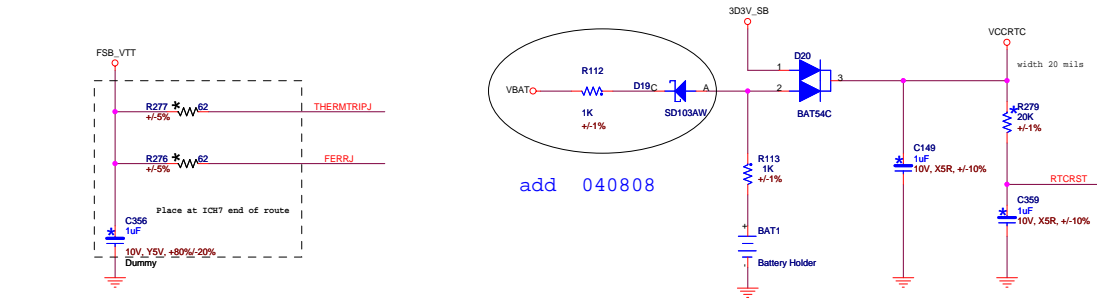




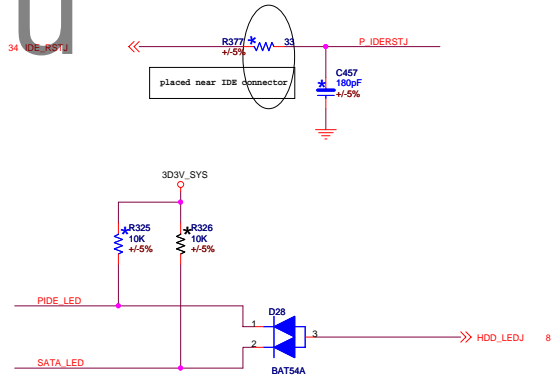
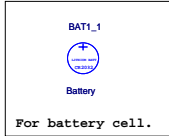
SATARBIA connection
5 mils width, length no longer than 500 mils
Trace tied together close to pins.

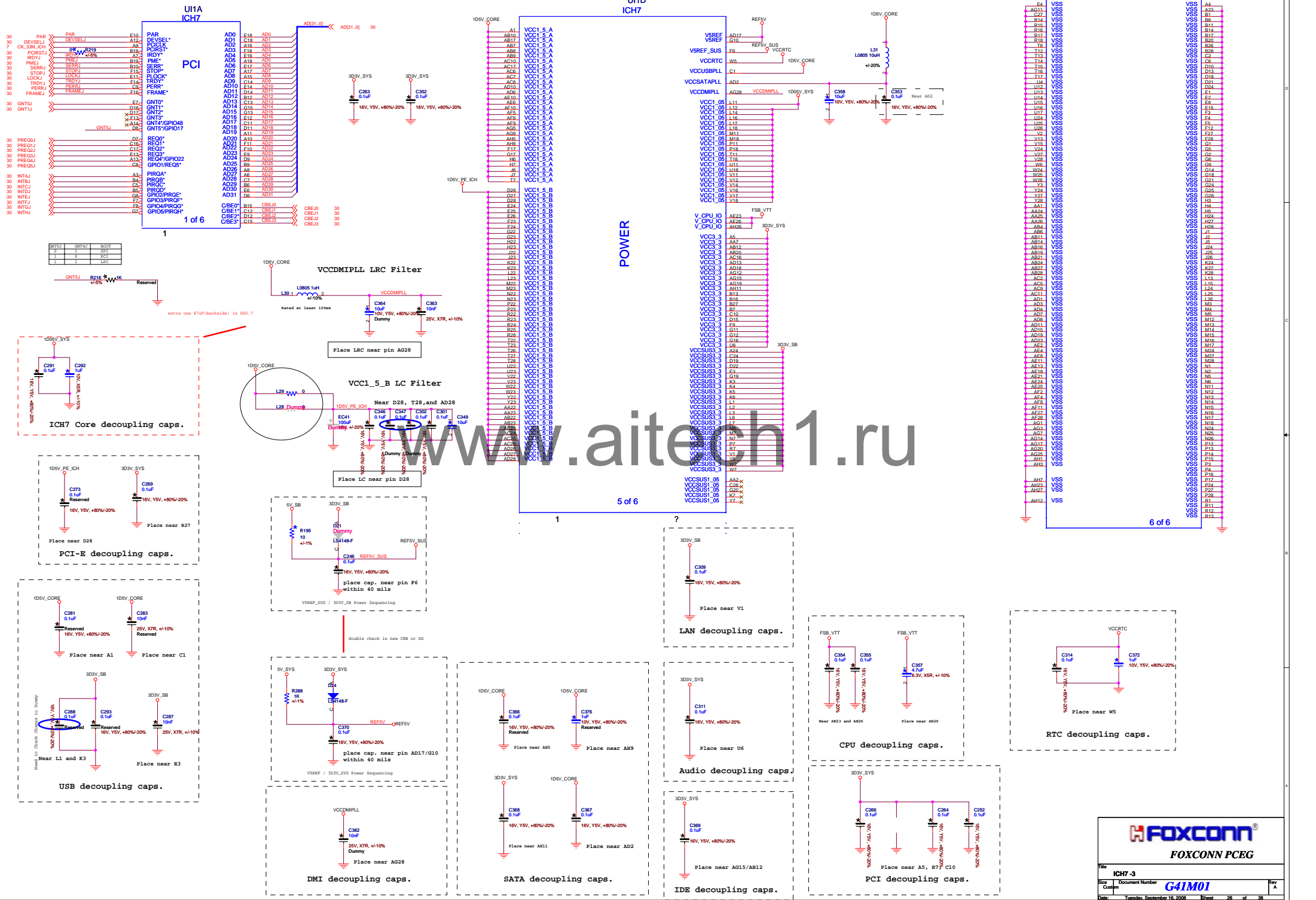


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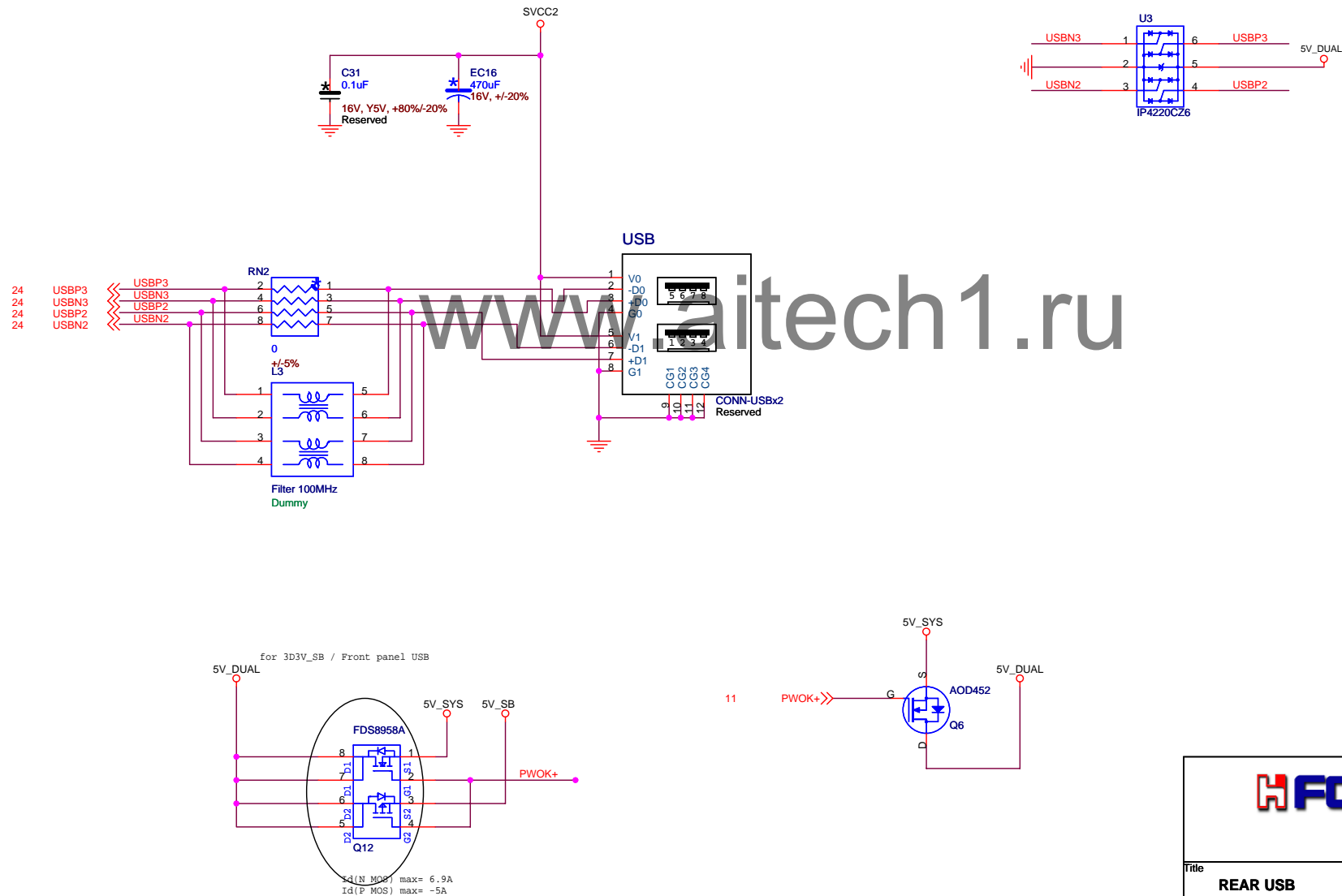


add 040808



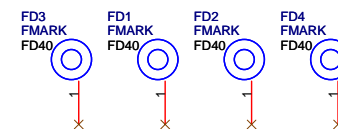
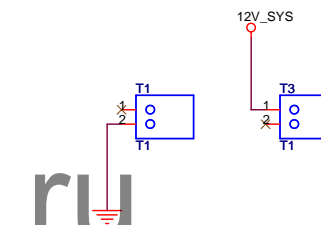
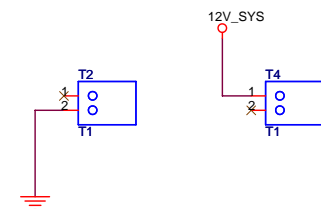
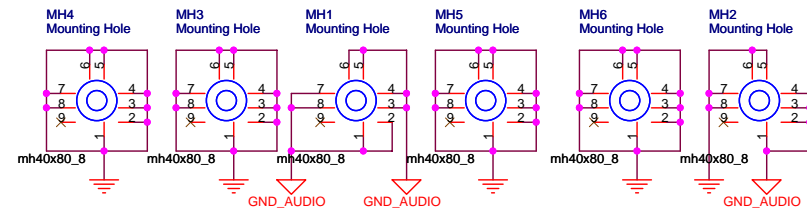
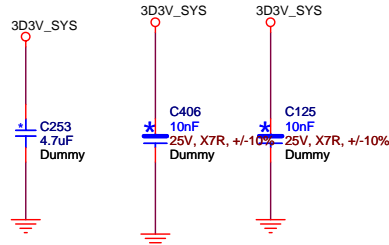
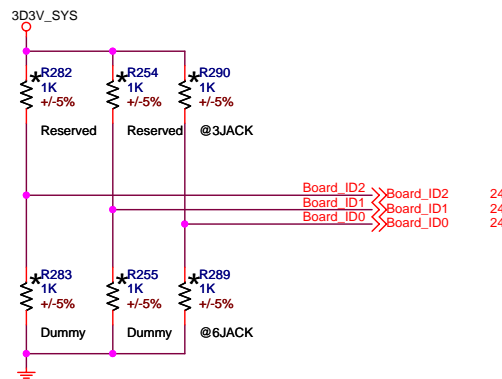


Rear Dual USB Connector

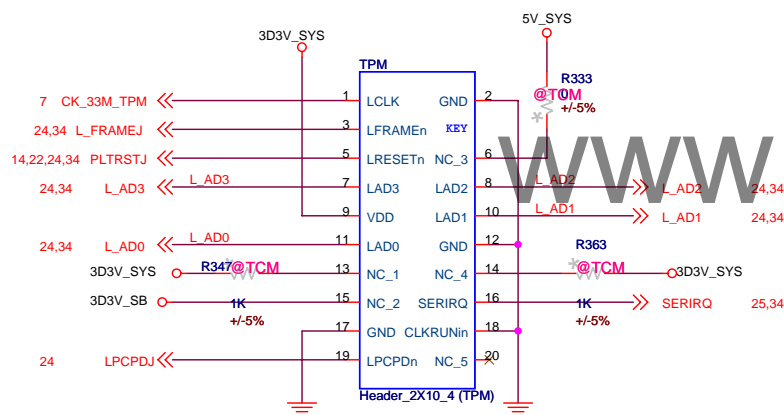


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TPM HEADER

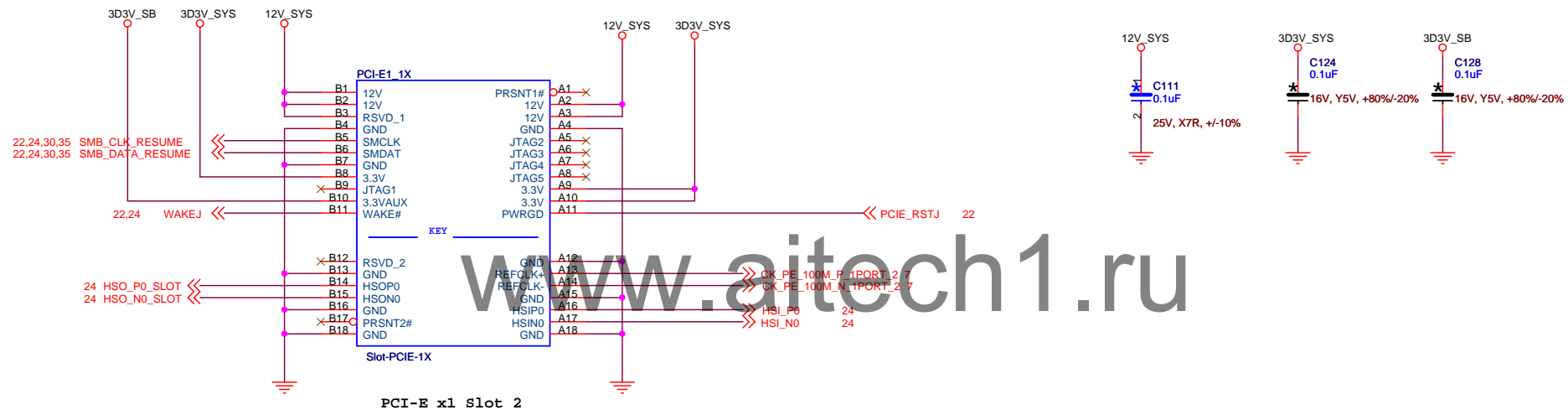


Need check?

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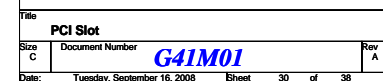
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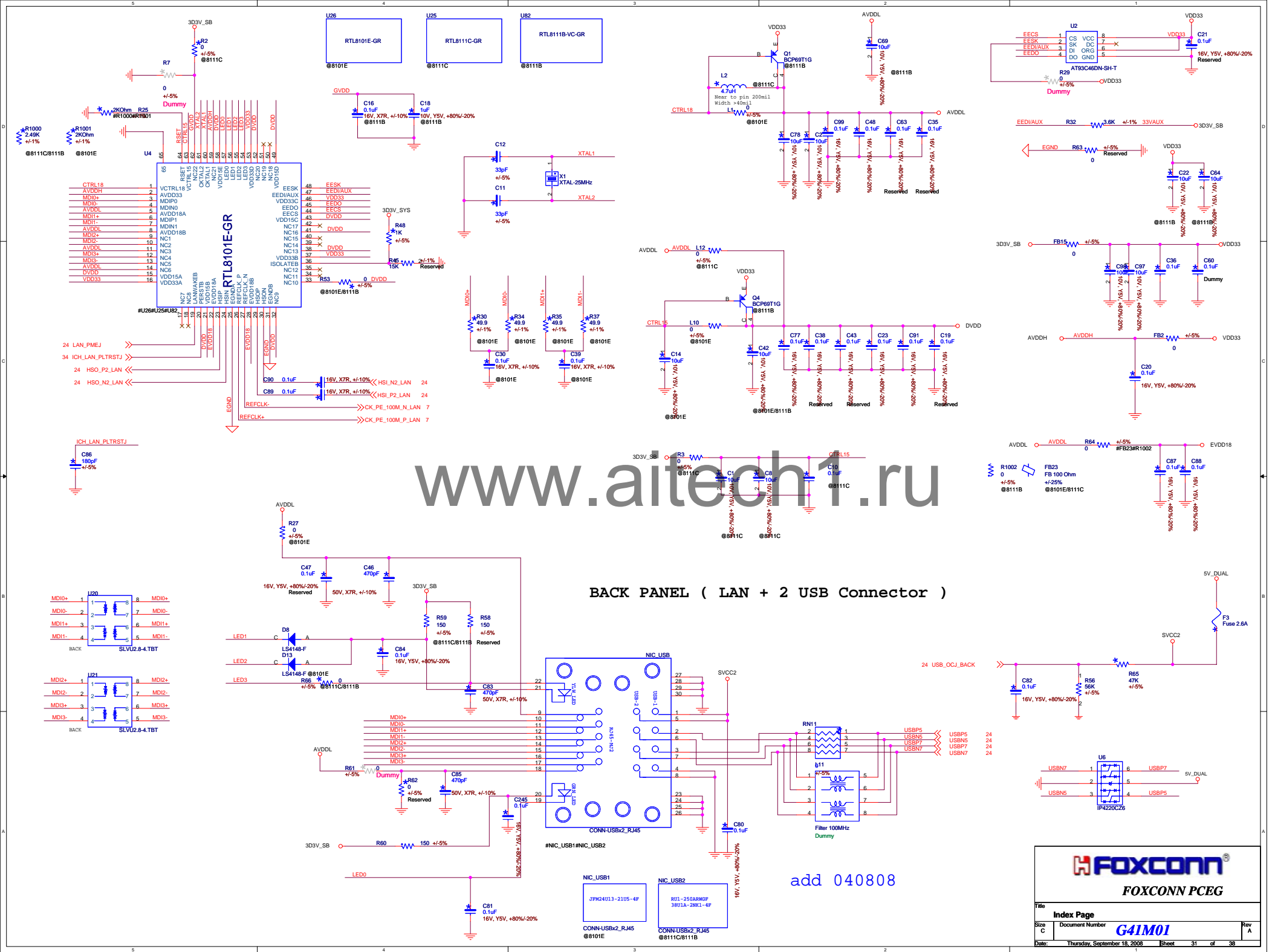
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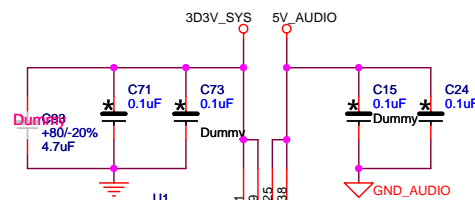
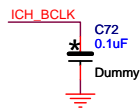
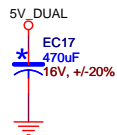
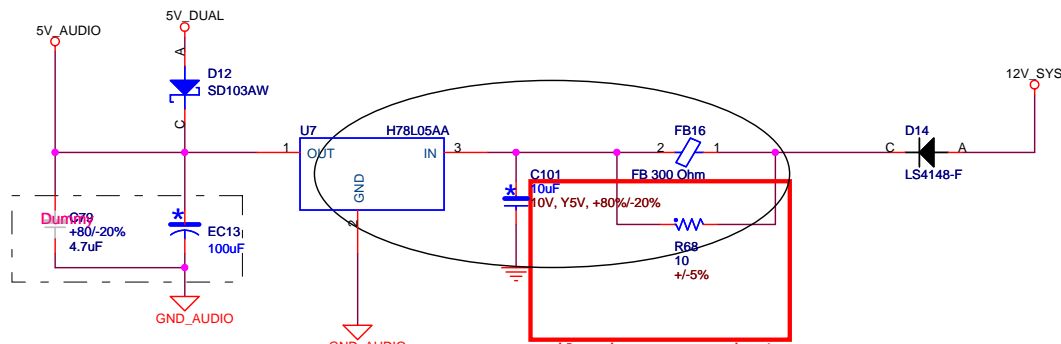


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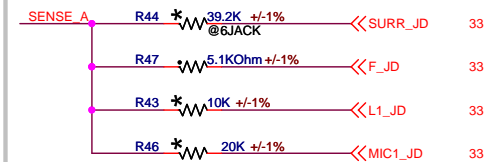
Title			
PCI Express x1 Slot			
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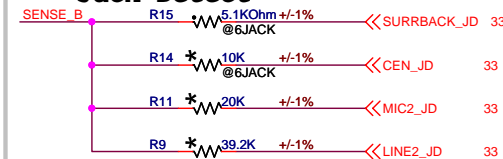




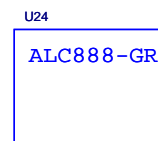
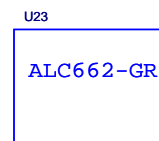
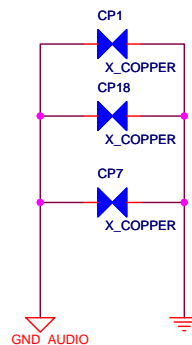
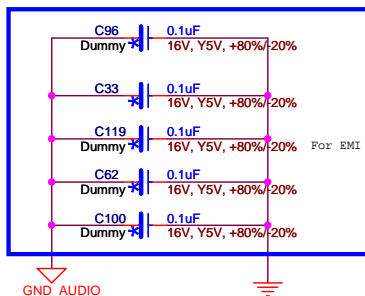
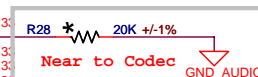
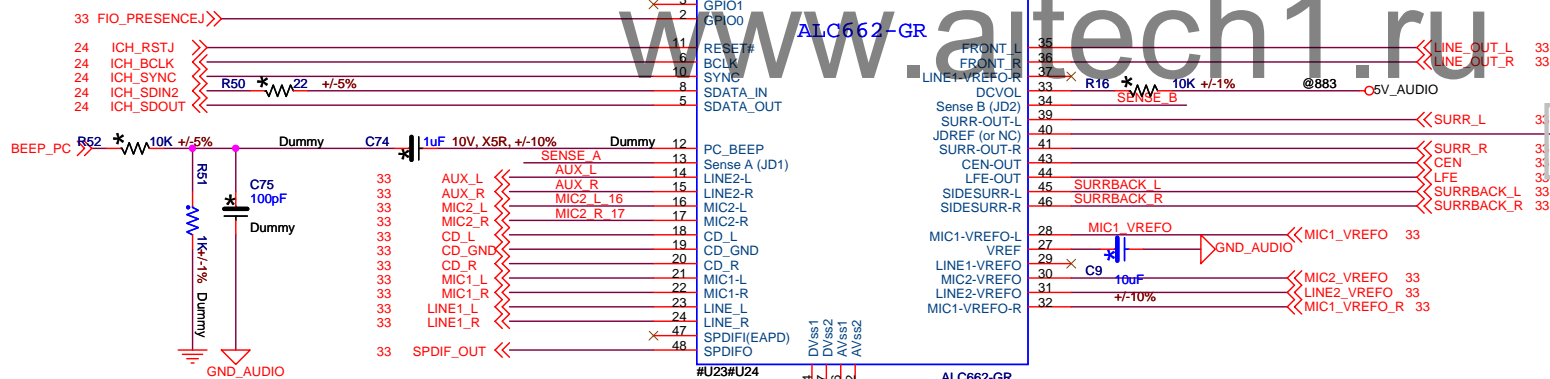
Jack Detect



Jack Detect



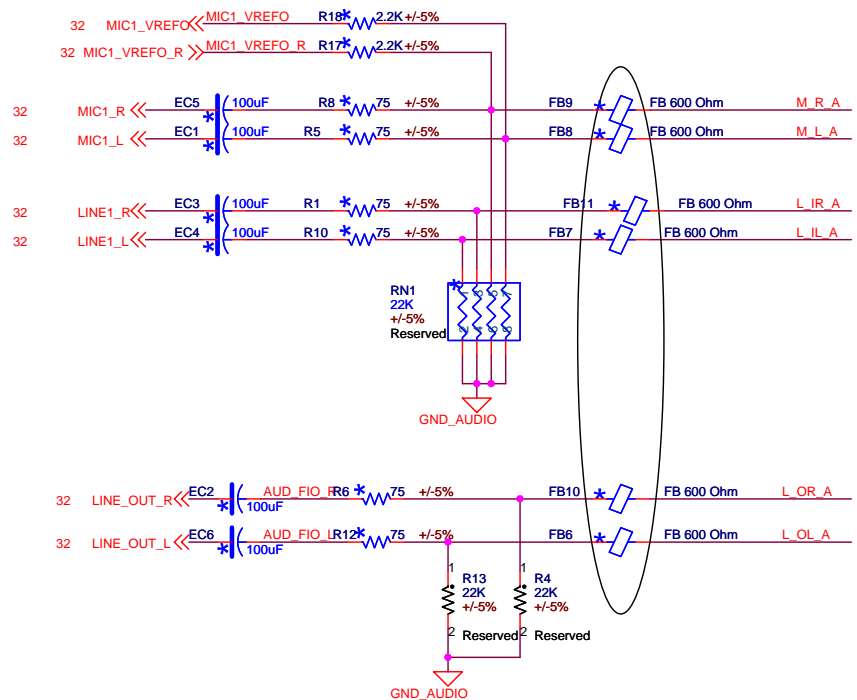
All of JD resistors should be placed as close as possible to Codec.



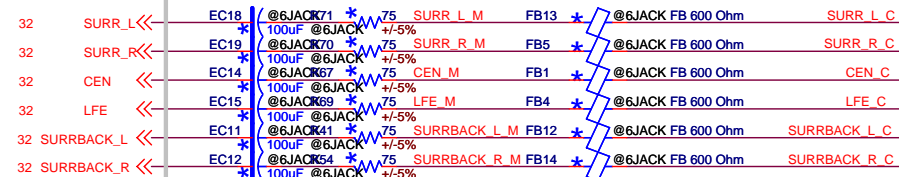
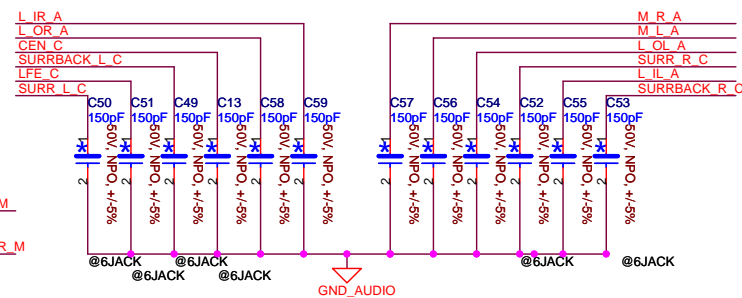
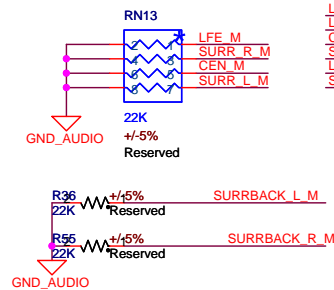
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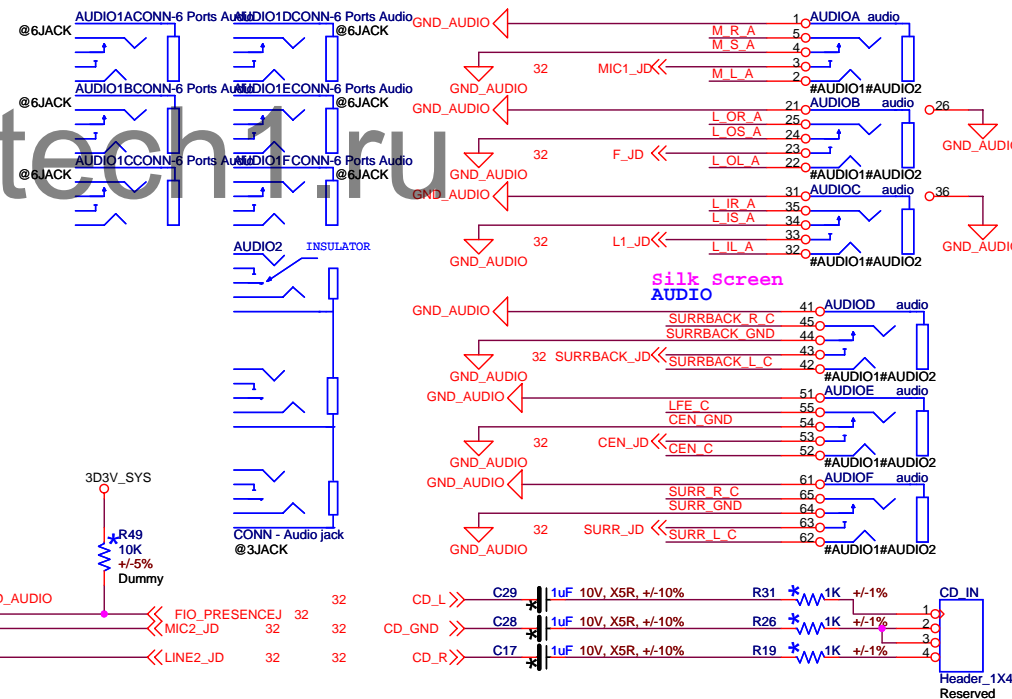
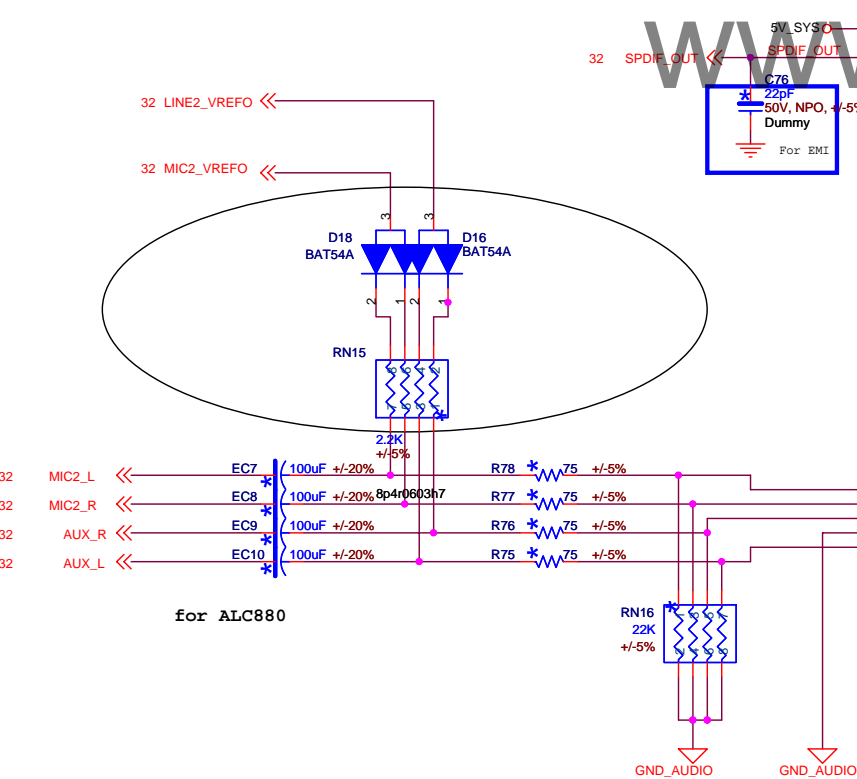
Title			
AUDIO 655/861			
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AUDIO
MIC-IN
AUDIO
LINE-IN

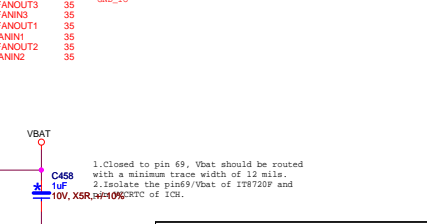
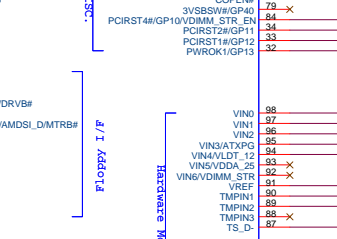
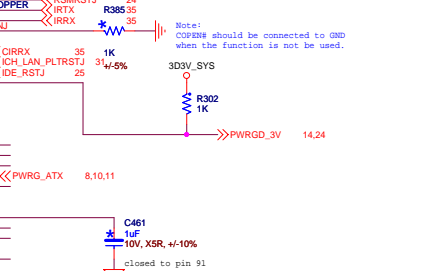
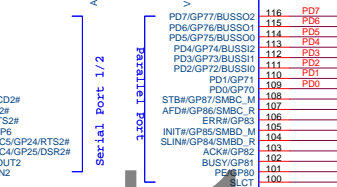
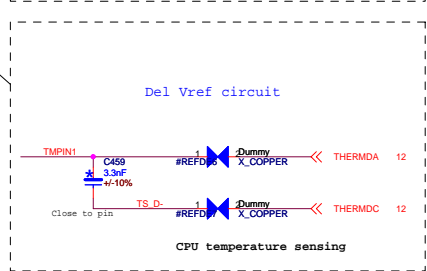
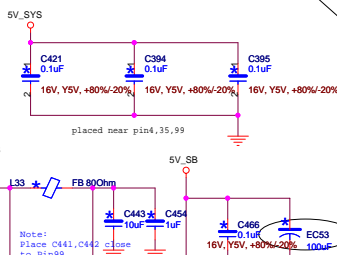
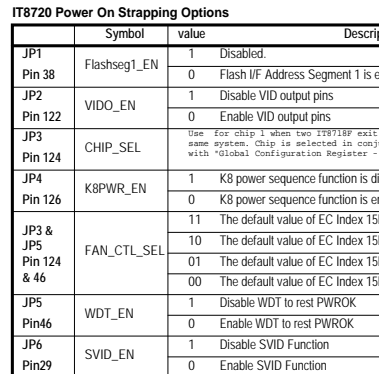


AUDIO
Front_OUT



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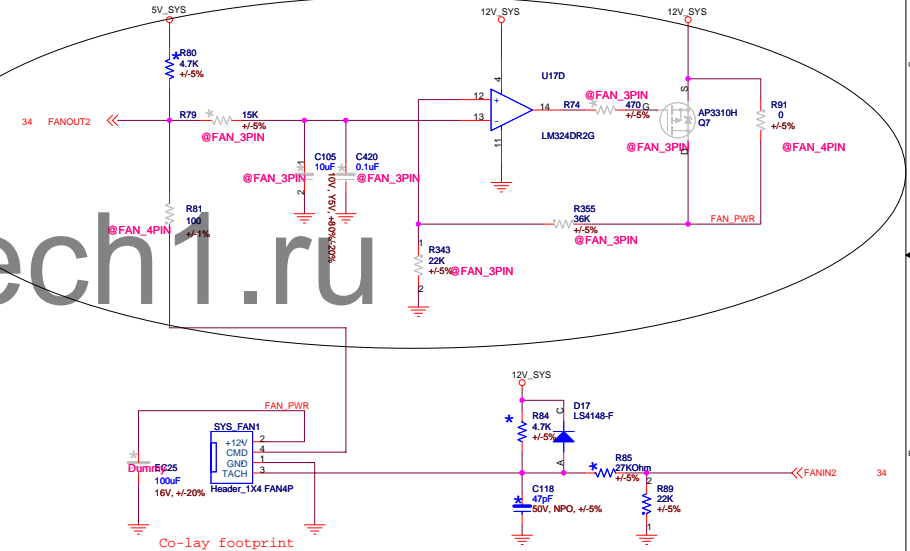
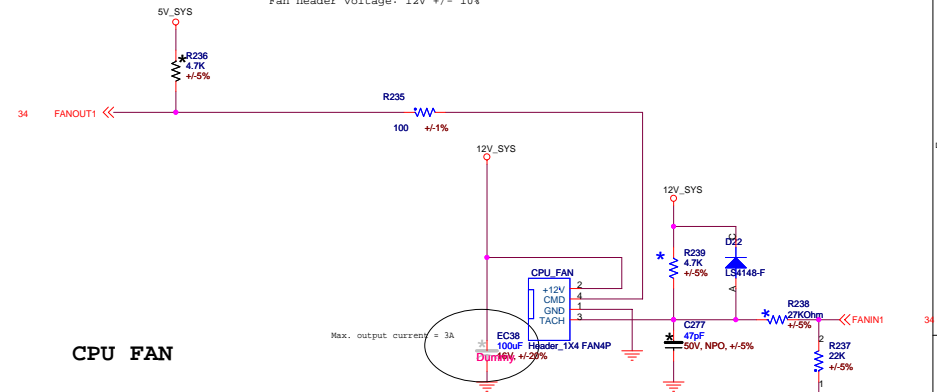
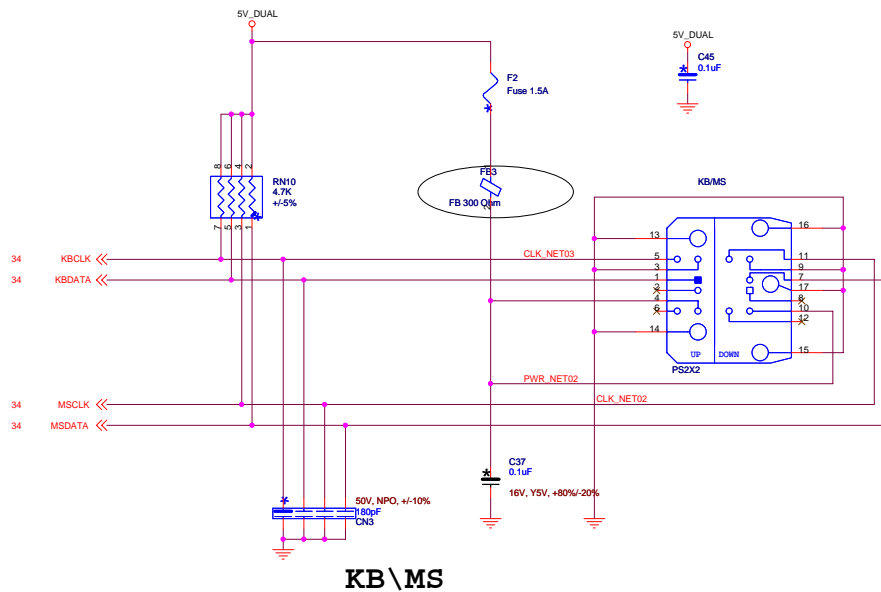
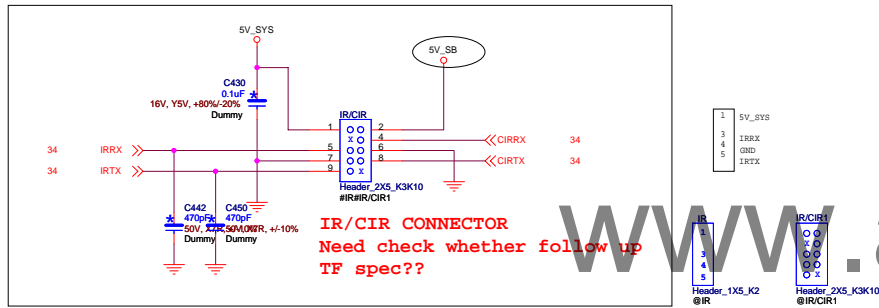
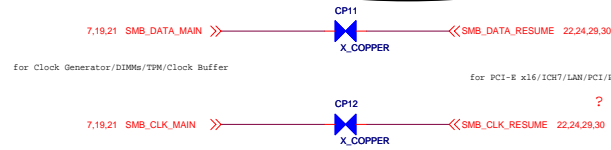
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<p align="center">FOXCONN PCEG</p>				
<p align="center">Super IO IT8720H</p>				
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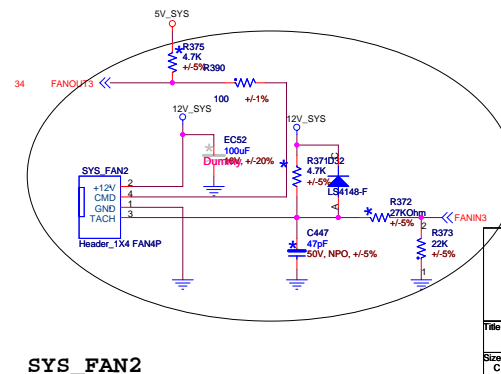
SM Bus Bridge

If use SUIO power good function, dummy Q7,Q6,Q8 pop R25,R18



Co-lay footprint

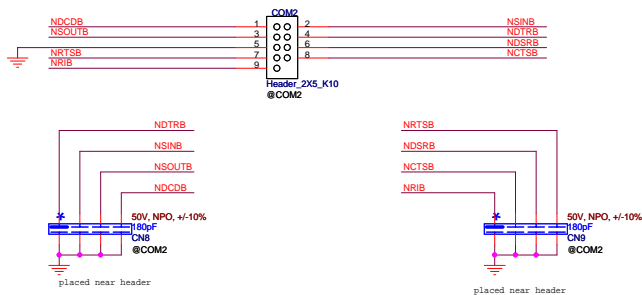
Max. output current = 3A



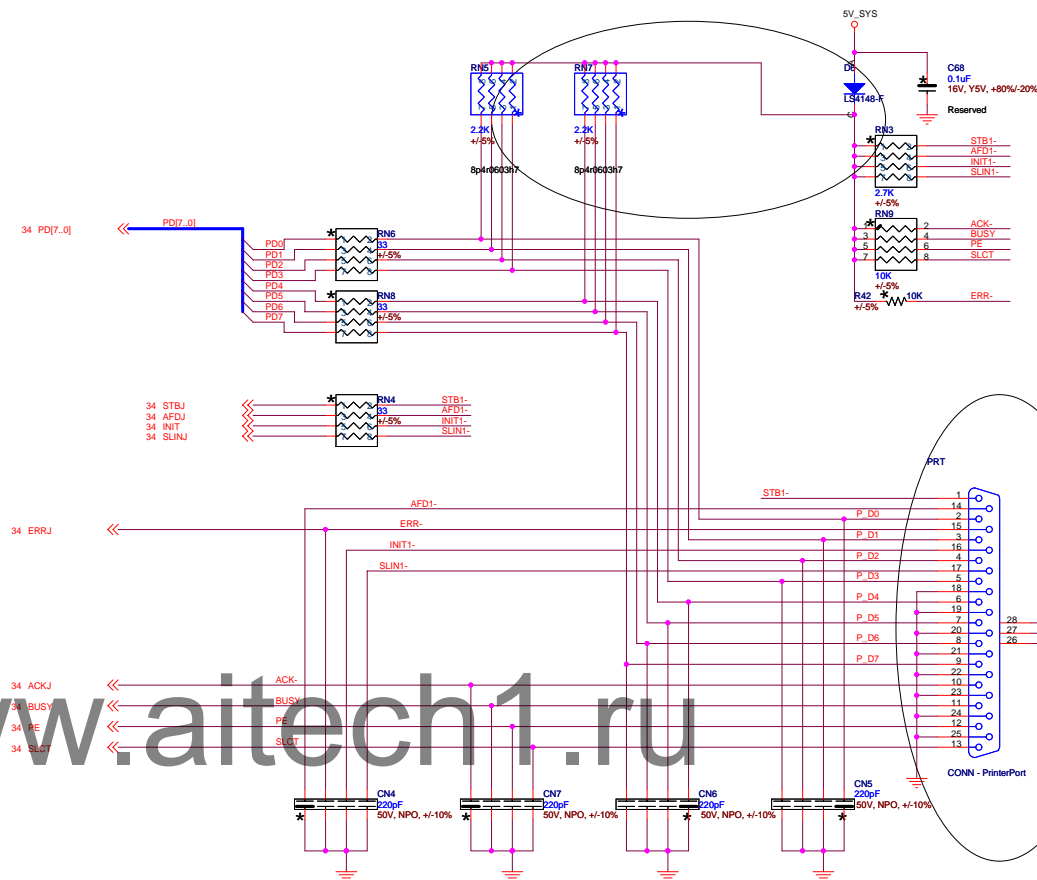
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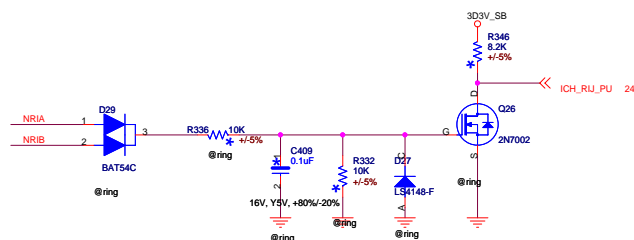
File		
Keyboard / Mouse / Fan		
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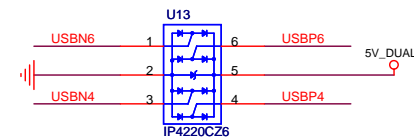
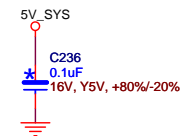
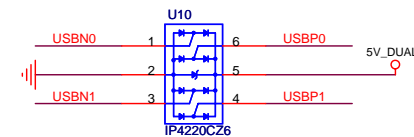
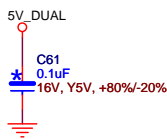
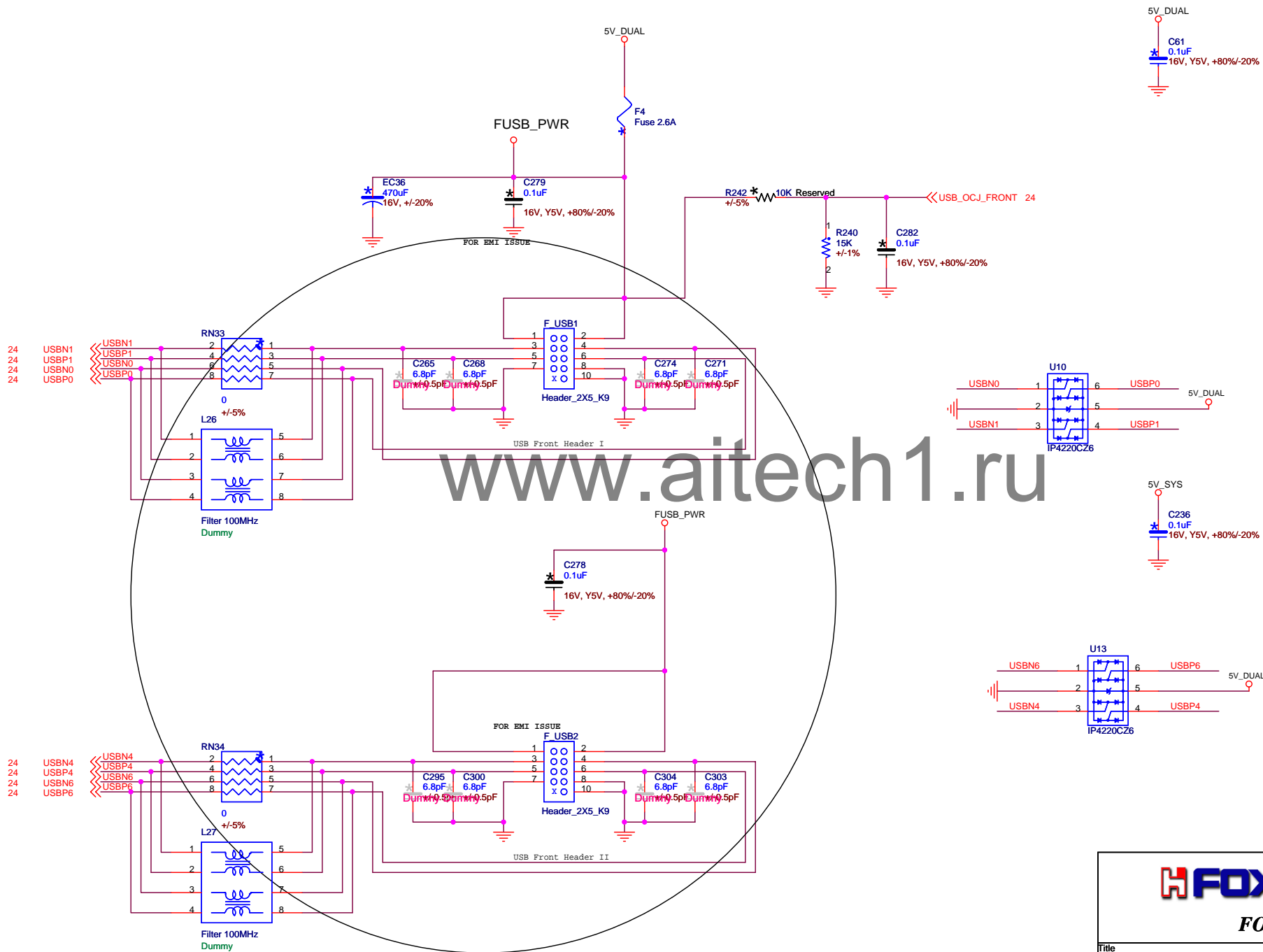
Timing diagram showing signals: ACK, BUSY, PE, SLEW. The signals are labeled with their names and a value of 34.



PRT PORT



Ring




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1. Change Lan RTL8111B colay RTL8101E to RTL8111C colay RTL8101E
2. Change Audio ALC888 colay ALC883 to ALC662 colay ALC888
3. Reserved Memory ratio schematic for over clock.
4. Del R108,C139,Q22,Q20,R107 and then connect VRMPWGD directly for VRD11.
5. Add R371,C501 for power button debounce circuit.
6. Reserved U15,U17 for TF spec.
7. Reserved TPM Header for TF spec.
8. Reserved U3,U6 for TF spec.
9. Add R8,R1,R5,R10,R6,R14,R87,R86,R85,R84,R78,R76,R73,R75,R41,R55 for Audio ESD
10. Reserved CIR function for TF spec.
11. Reserved NB FAN.
12. Reserved C307,C314,C324,C318,C348,C350,C360,C357 for TF Front Panel
13. Change R335 to 91ohm,R337 to 115ohm for Memory Power
14. Remove R338 and stuff R332 for FAN half speed when Power on.
15. Reserved R46 for realtek's suggestion
16. Reserved U9,C144,C145 for VCCA_DAC
17. Add RT8111B SCH
18. Del EC72,EC55,EC54,EC73 for placement issue
19. Reserved R40,R25 For EMI
21. Add C16,C17 For RTL8111B LAN Chip EMI
22. Add FB22 For ITE suggestion
23. Reserved C497 for Front Panel ESD
24. Del Power V15SFR SCH
25. Add R208,R220 for further CPU
26. Reserved R321,R109,R320 for PCI RST
27. Disconnect SLP_S4 with CLK Gen
28. Change C368,C371 from 18pF to 12pF
29. Change F_AUDIO Pin7 connect to Audio_GND directly and connect Pin6,Pin10 to codec through the resistor.
- After Gerber Out:
30. Reserved C506
31. Change R363 size from 0402 to 0603
32. Change R111 to 33ohm 1%
33. Add R400 100ohm 1%
34. Dummy Q24 C146
35. Reserved R94 In 8KS2H SKU
36. Reserved R114,C147,R110,Q23,Q26
37. Change R116,R118 to 10K 1%
38. Change C160 to 1uF 0603
39. Reserved Q39
40. Del CP2
41. Del EC29
42. Reserved R356
43. Change PCIe_16x slot to 2EG48211-S7Y-4F
44. Del EC65,EC66
45. Add EC68
46. Change L25,L38 to 630307400-176-G
47. Reserved C451,C396,C375,C381,C430,C441,C355,C436,C447,C448,C397,C385,C446,C427,C405,C401,C395,C353,C390
48. Del RN17
49. Add R401,R402,R403 10K 5%
50. Add JP1,JP2, JP1(P1&P2),JP2(P1&P2)
51. Add R404 470ohm
52. Add EC69
53. Del EC46,EC47
54. Change L26,L37 to APL1108P-2R5L
55. Change C5,C6,C7 to 10pF
56. Change L8,L9,L10 to GL1608082NJT
57. Reserved C38,C65
58. Change CP14 to L40 10uH
59. Change L23 to 10uH
60. Add C139,C513,C514 10uF
61. Add EC65
62. Del CP24
63. Add R25 for EMC
64. Add R409,R410,R411 for Audio codec ESD protection
65. Change EC55 to 680uF
66. Change L23 from 10uH to 10ohm

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CHANGE LIST		
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